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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gene Chui

Serial No. 09/090,096

Filed: June 3, 1998

For: A METHOD AND APPARATUS FOR PROVIDING PROGRAMMABLE MEMORY FUNCTIONS FOR BI-DIRECTIONAL TRAFFIC IN A SWITCH PLATFORM

EXAMINER: LOGSDON, JOSEPH B.

ART UNIT: 2662



Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

**SUBMISSION OF FORMAL DRAWINGS**

Enclosed for filing in the above-referenced patent application are forty five (45) sheets of formal drawings.

Respectfully submitted,

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Dated: 1/13, 2005

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Signature

1/13/05
Date

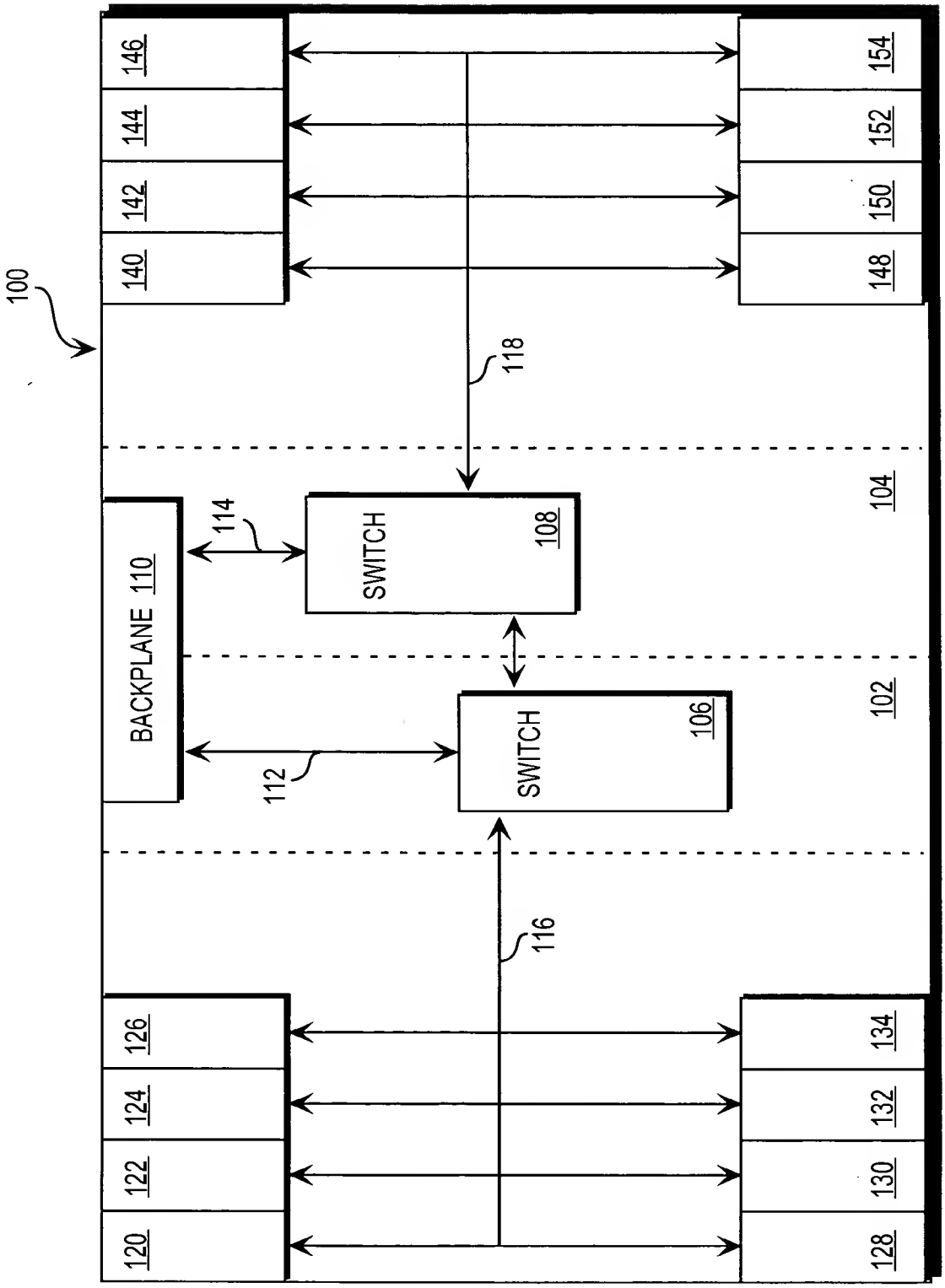


FIG. 1

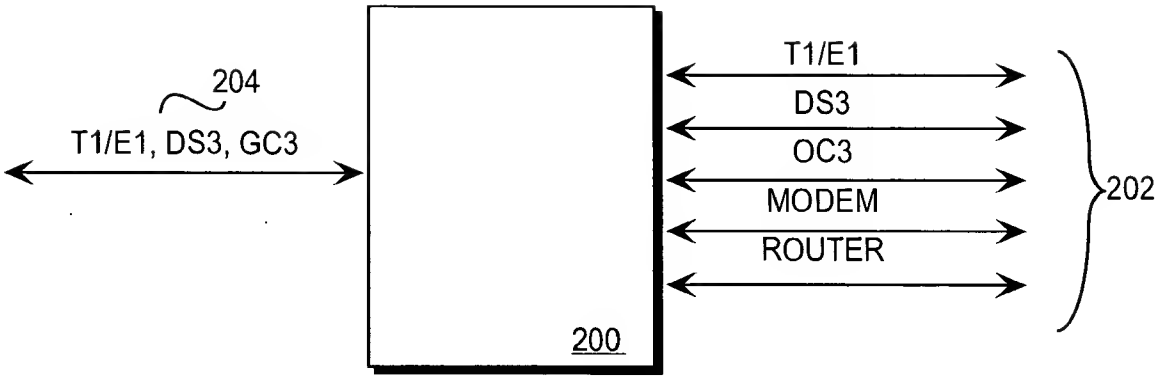


FIG. 2

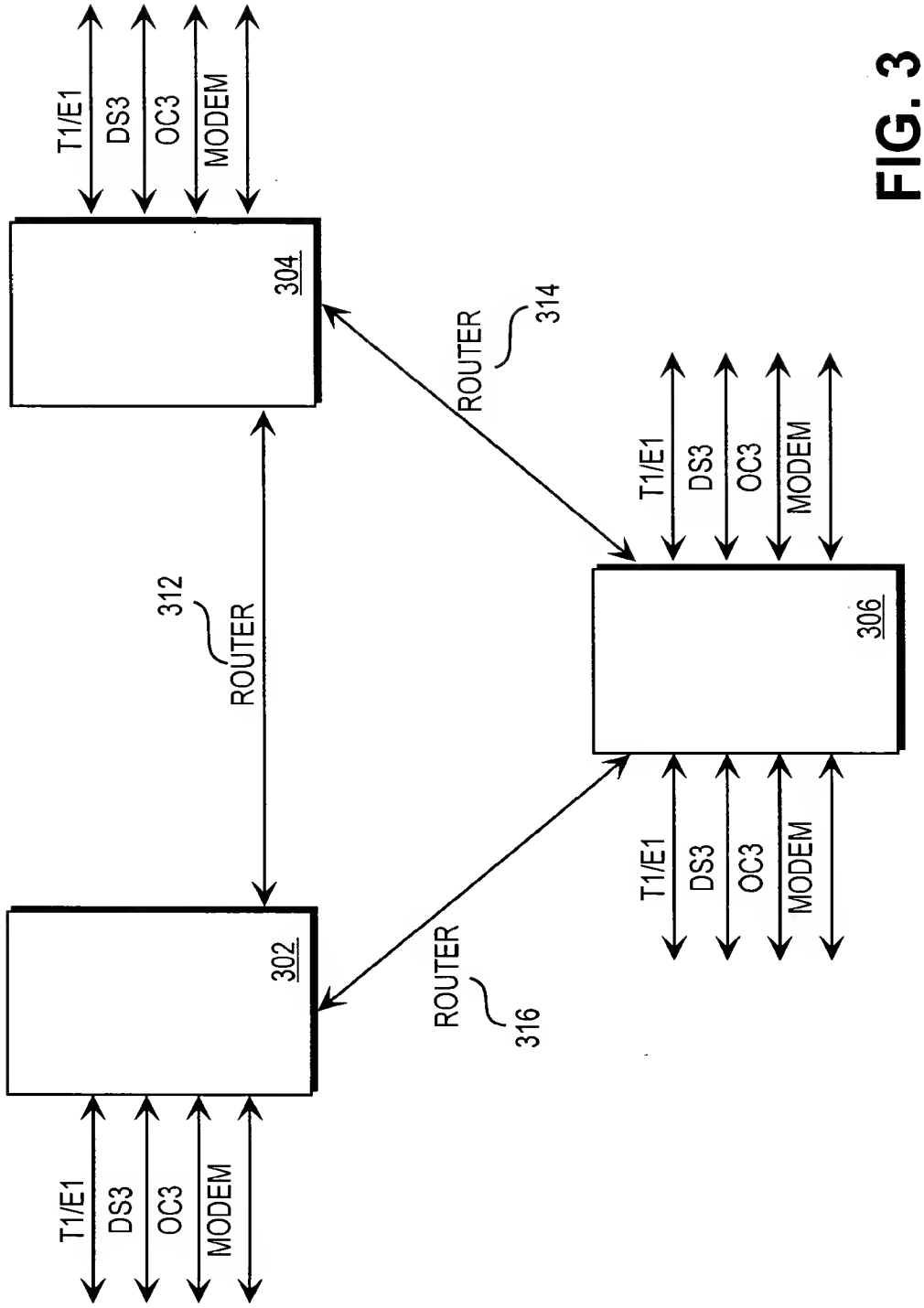


FIG. 3

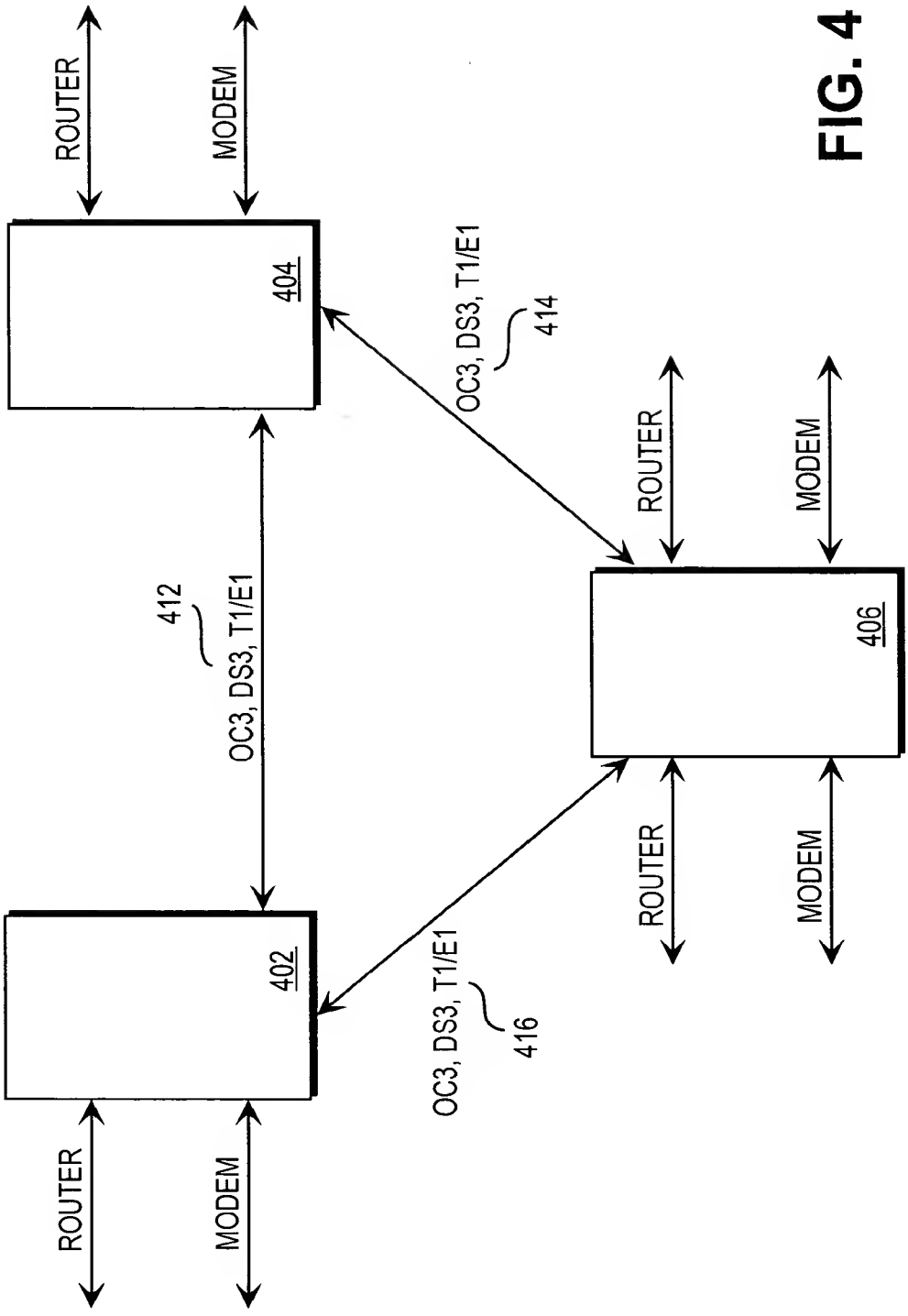


FIG. 4

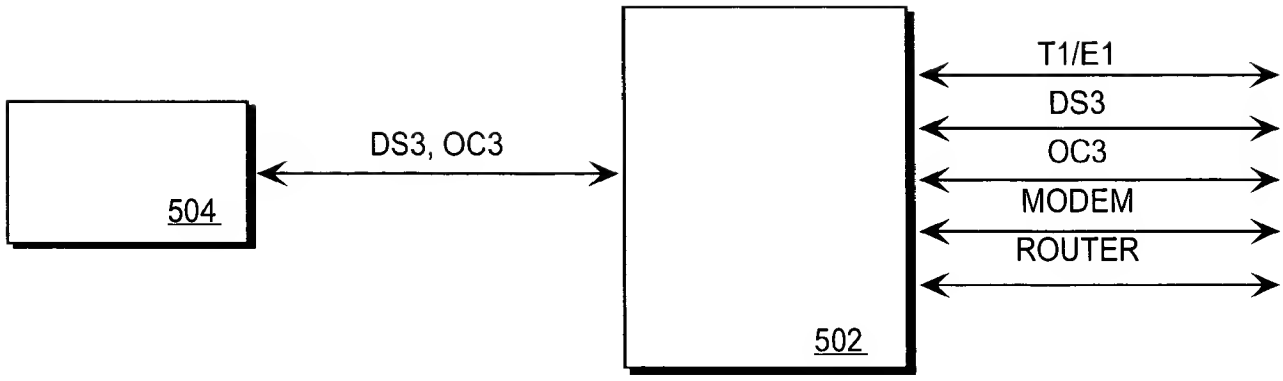


FIG. 5

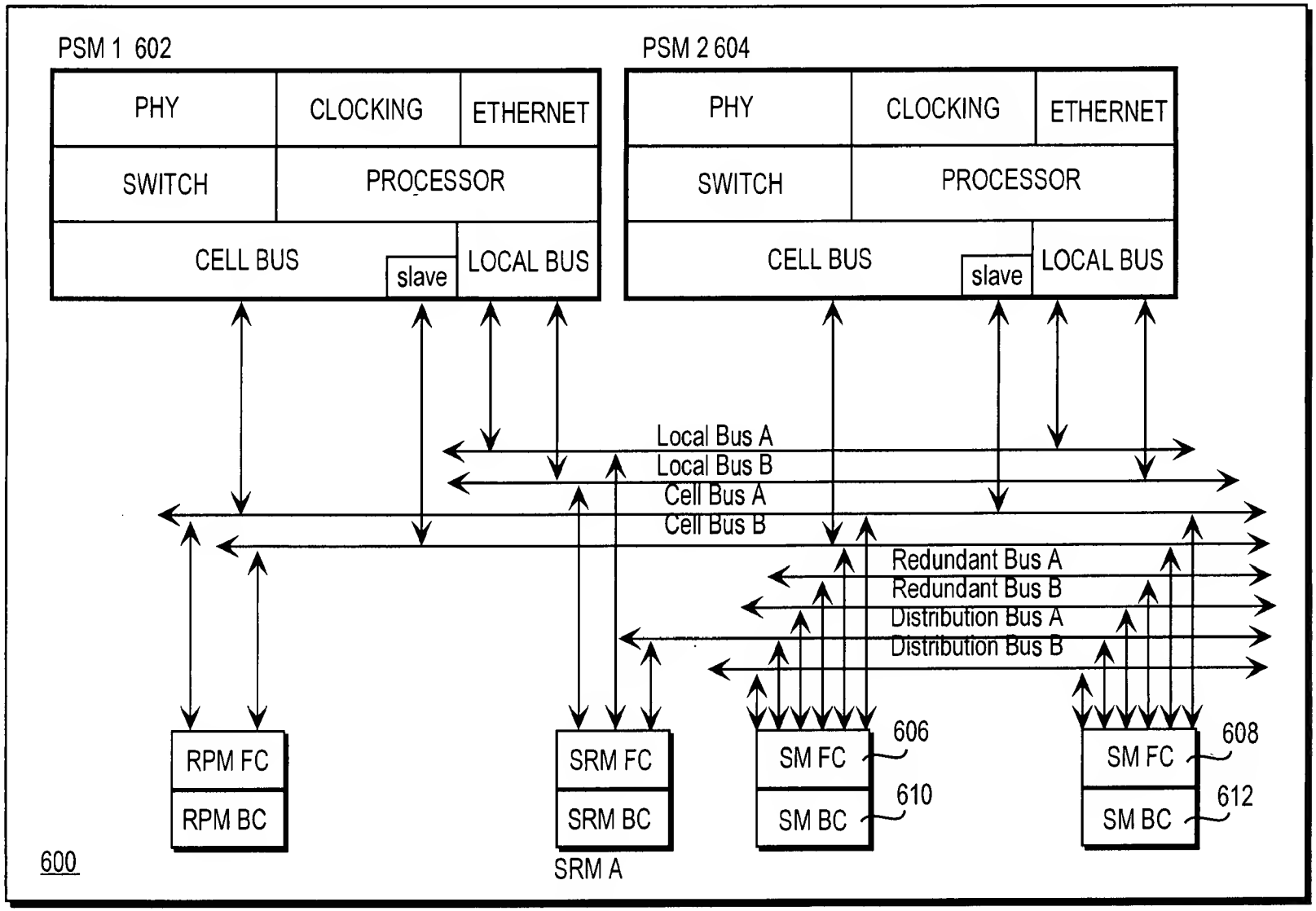


FIG. 6

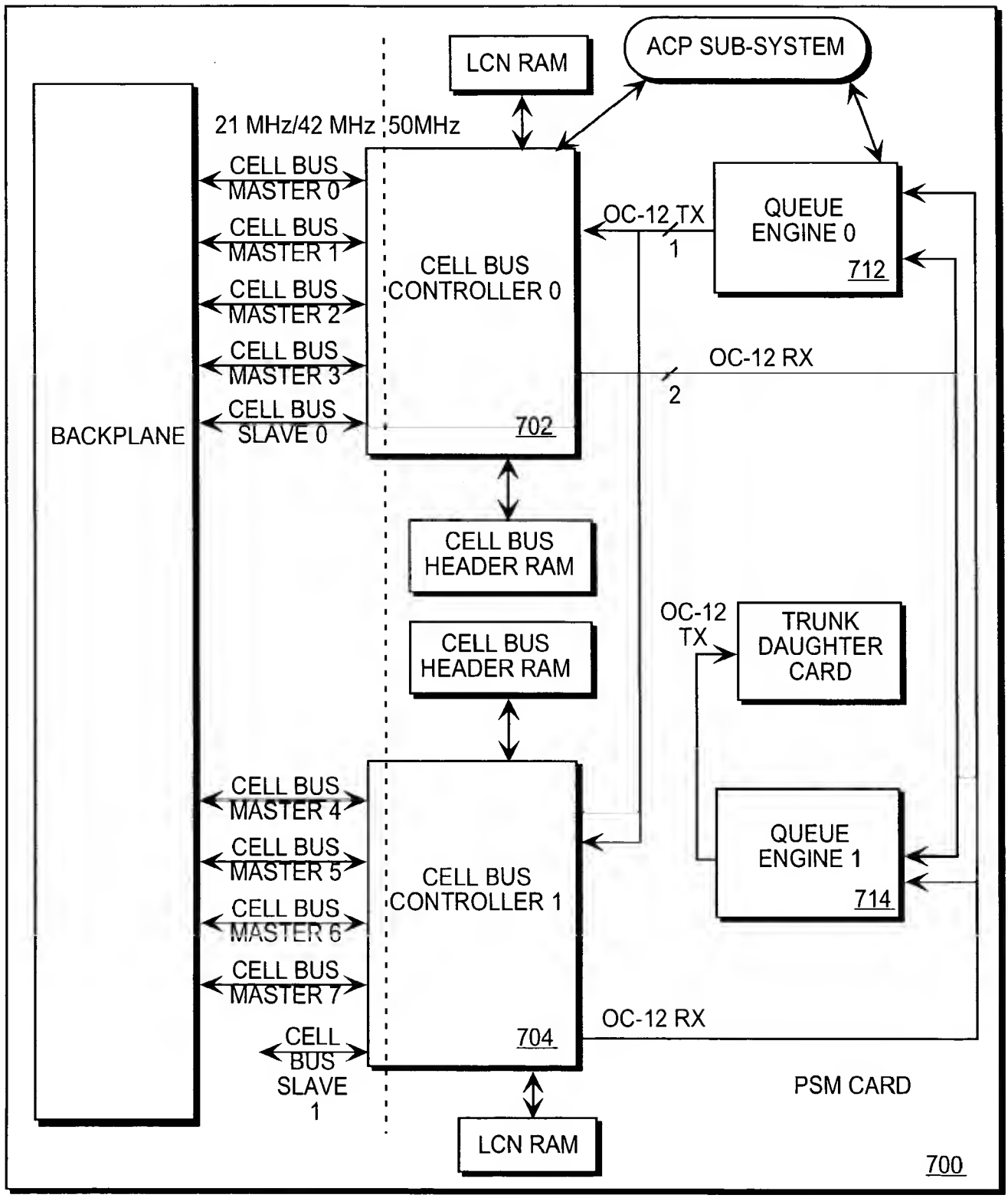


FIG. 7

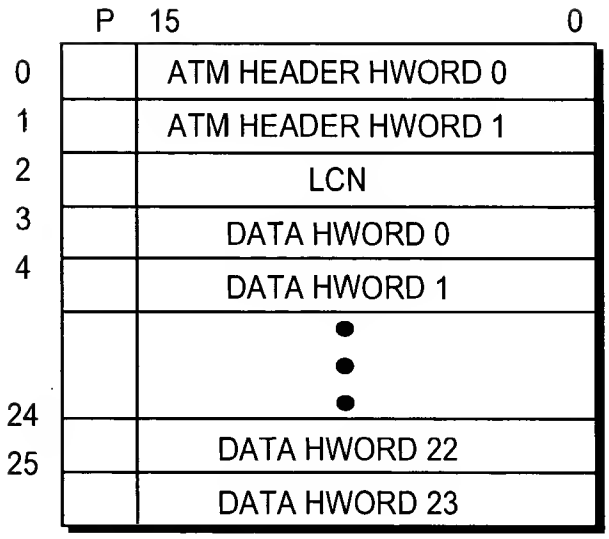


FIG. 8

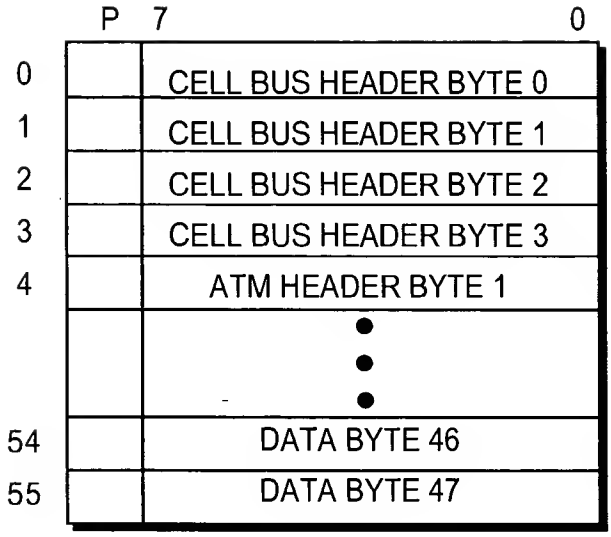


FIG. 9

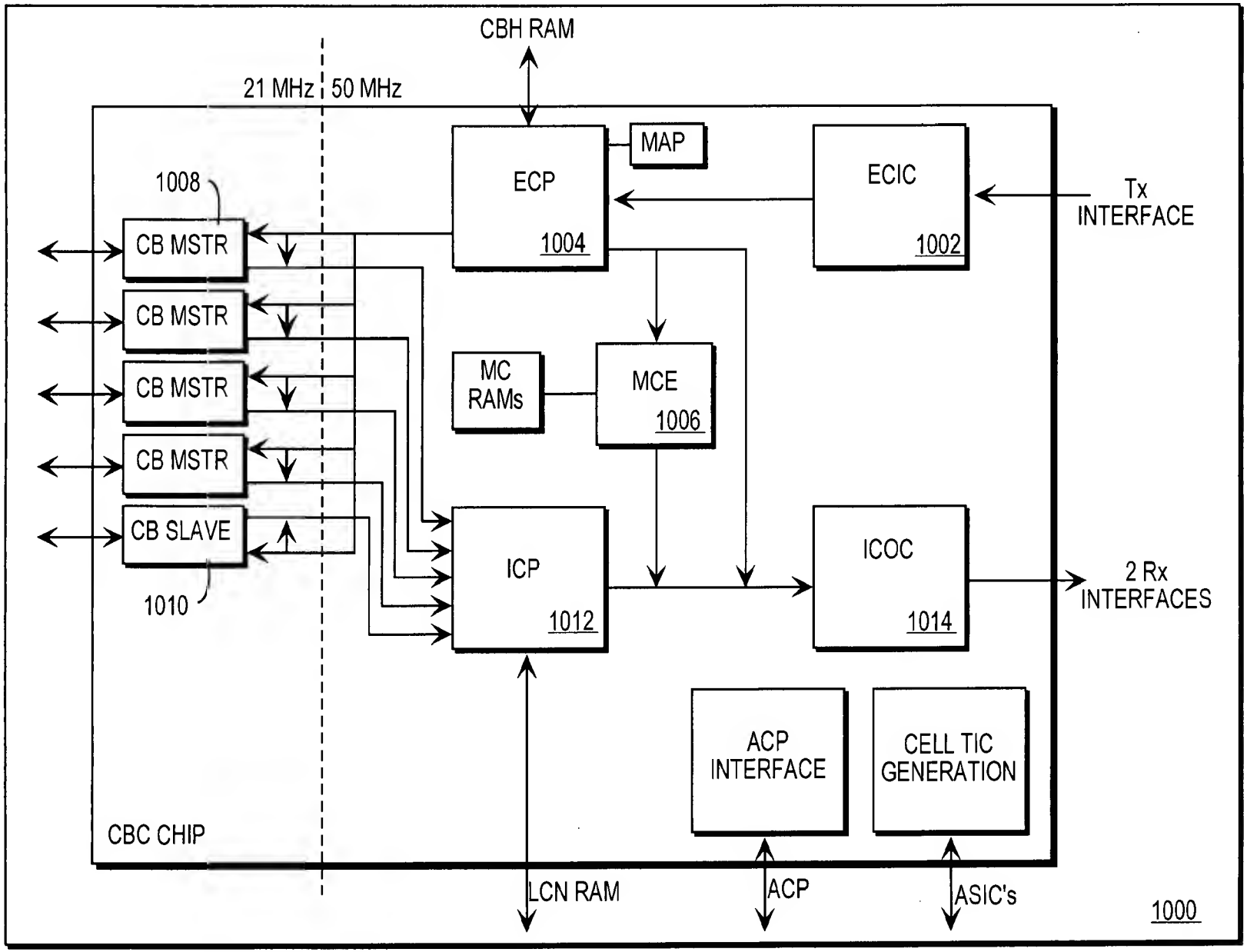


FIG. 10

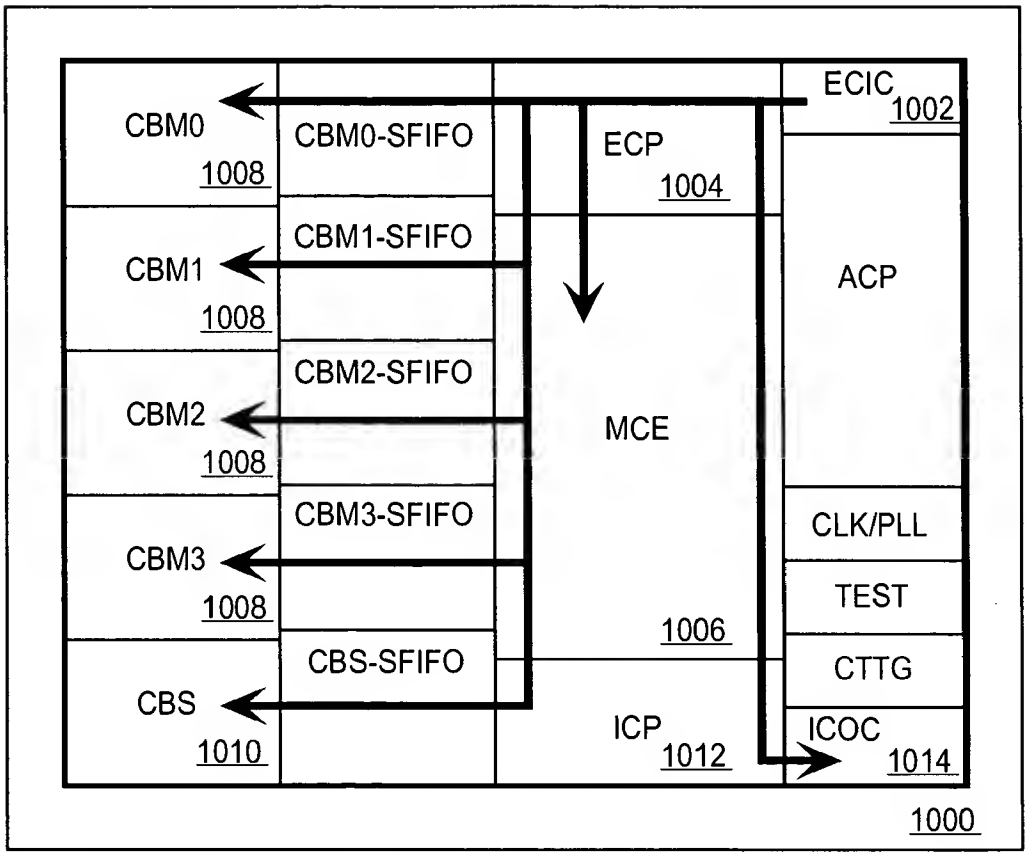


FIG. 11

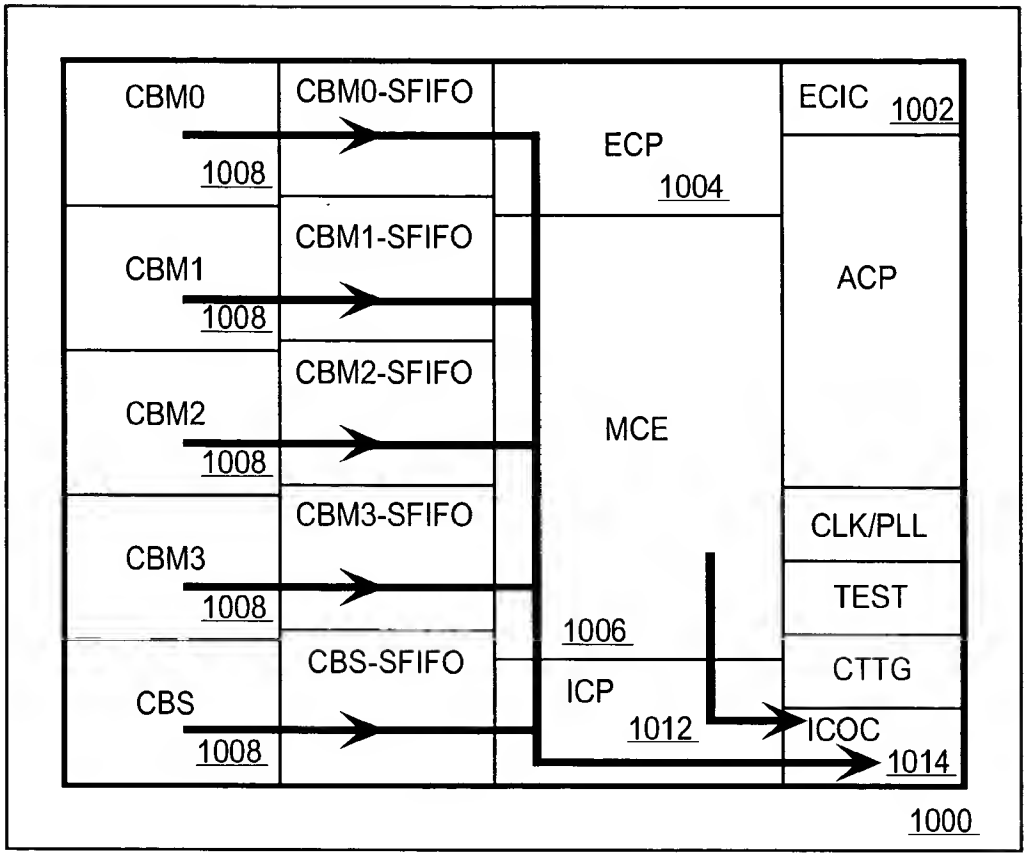


FIG. 12

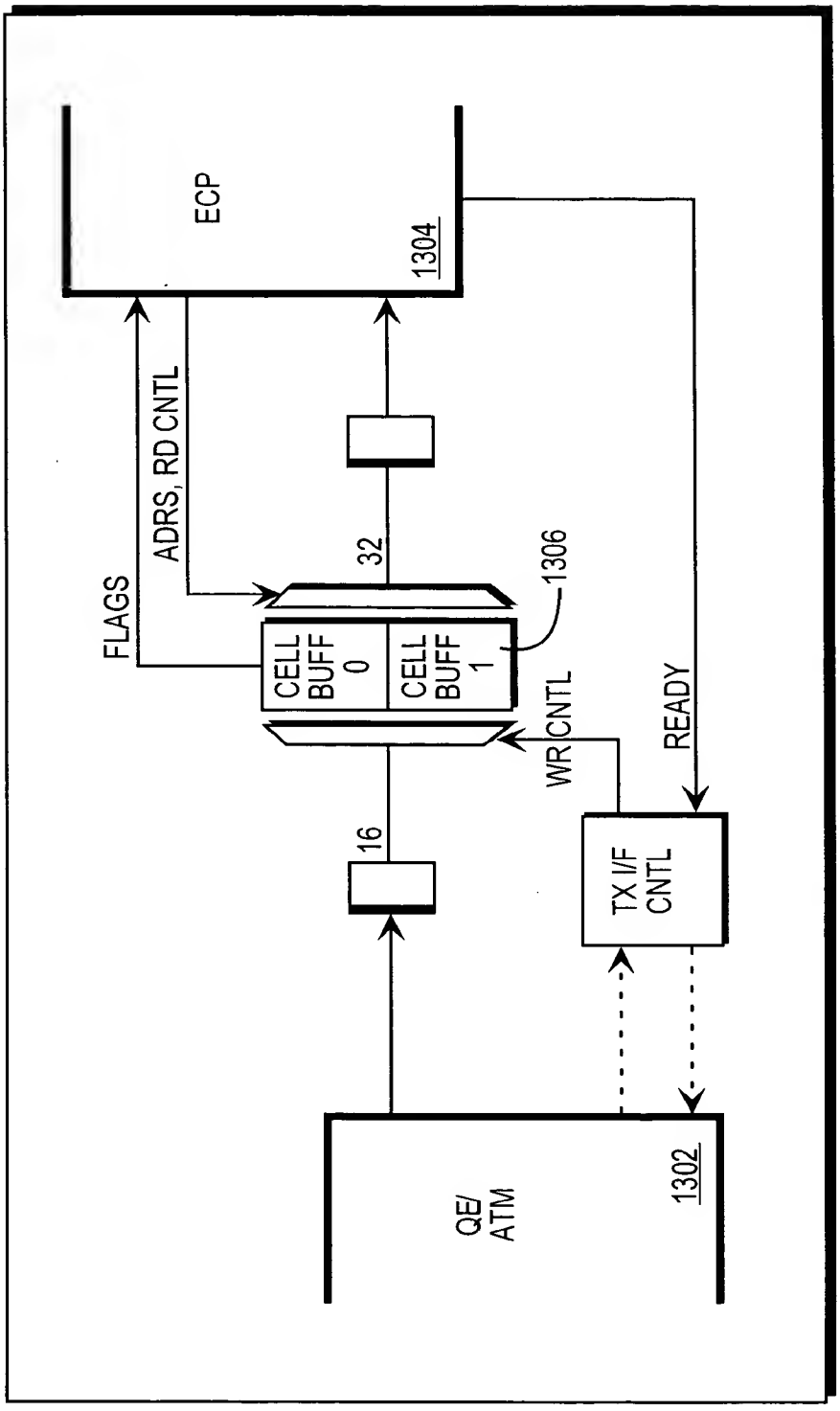


FIG. 13

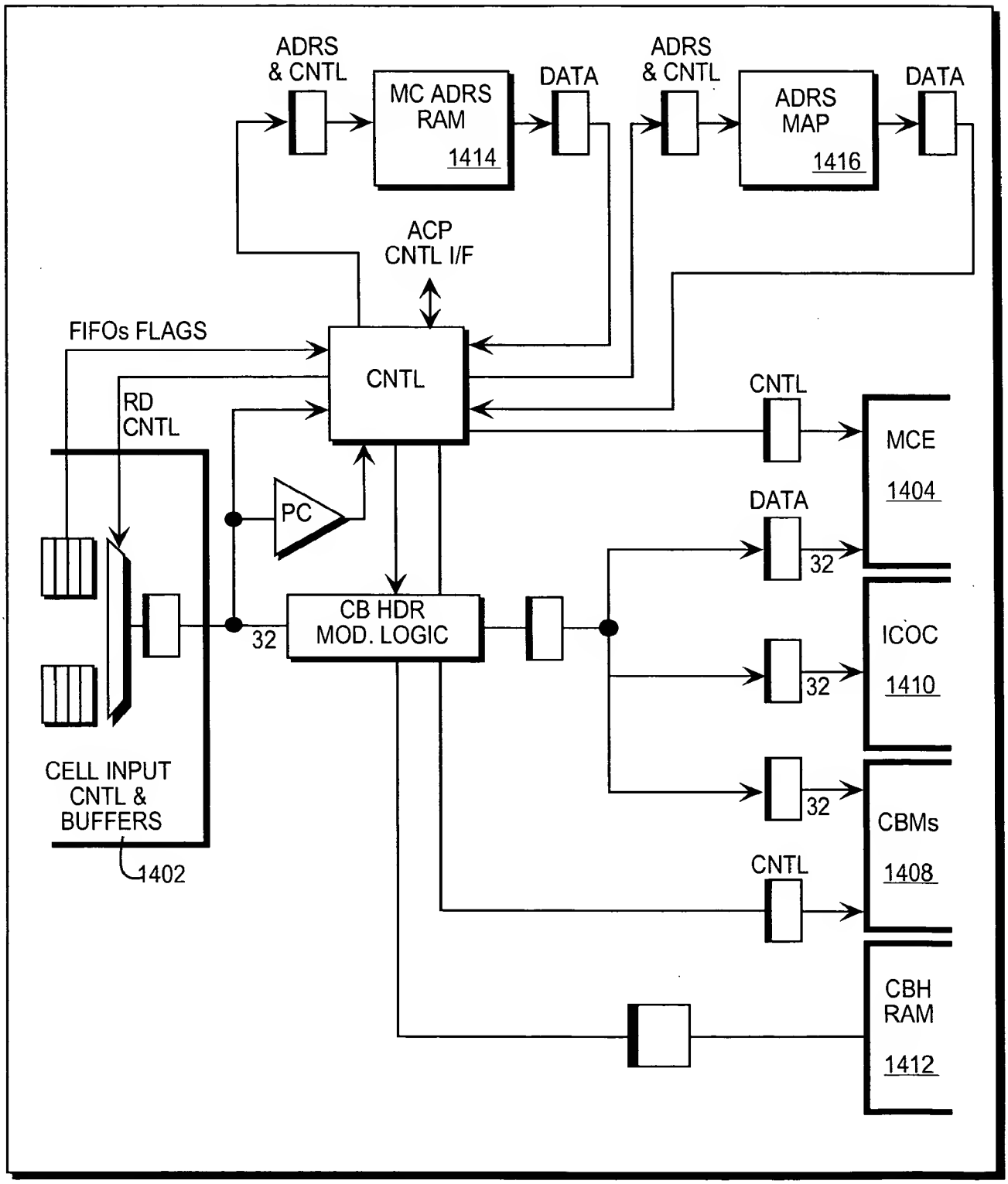


FIG. 14

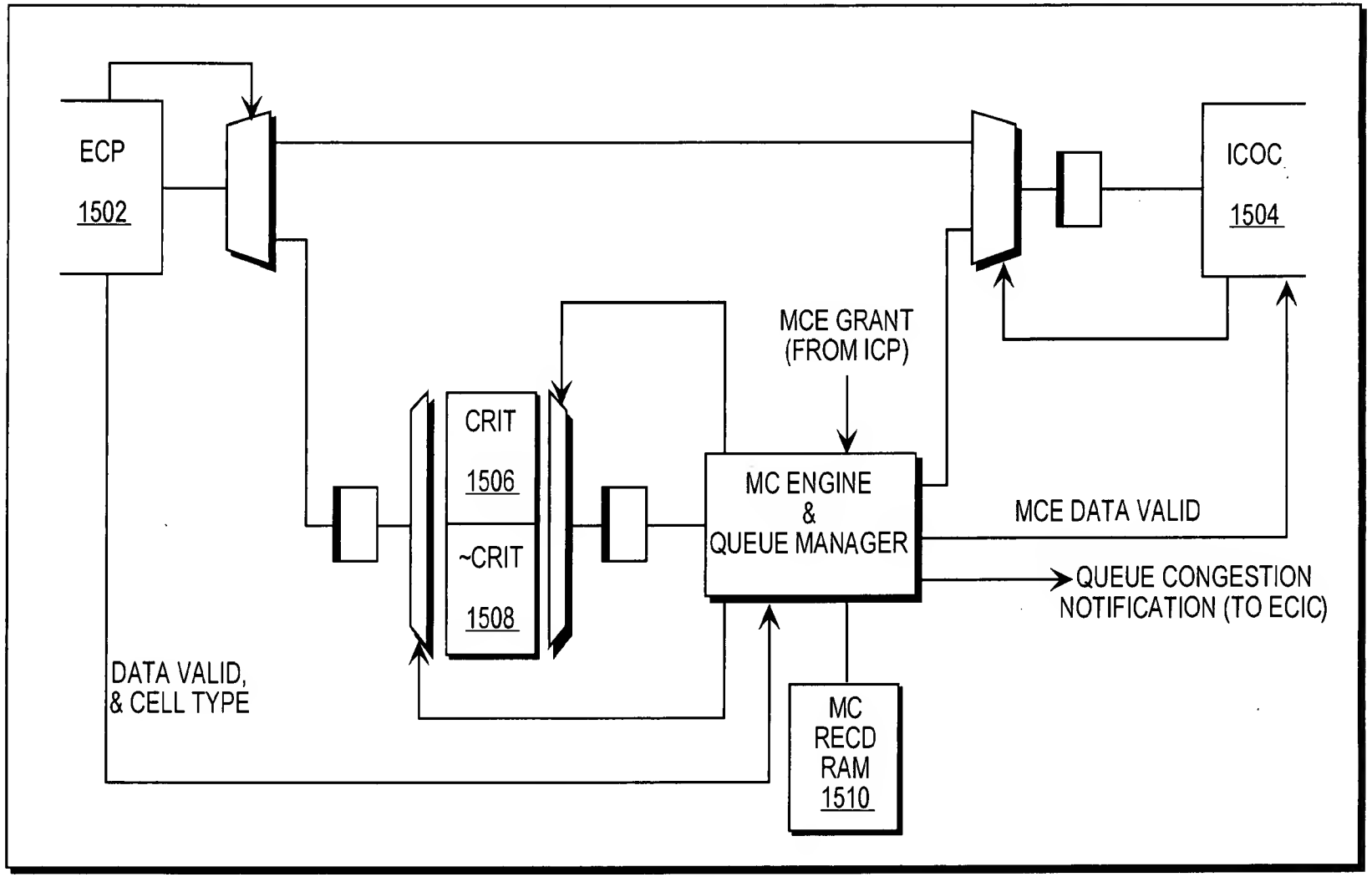


FIG. 15

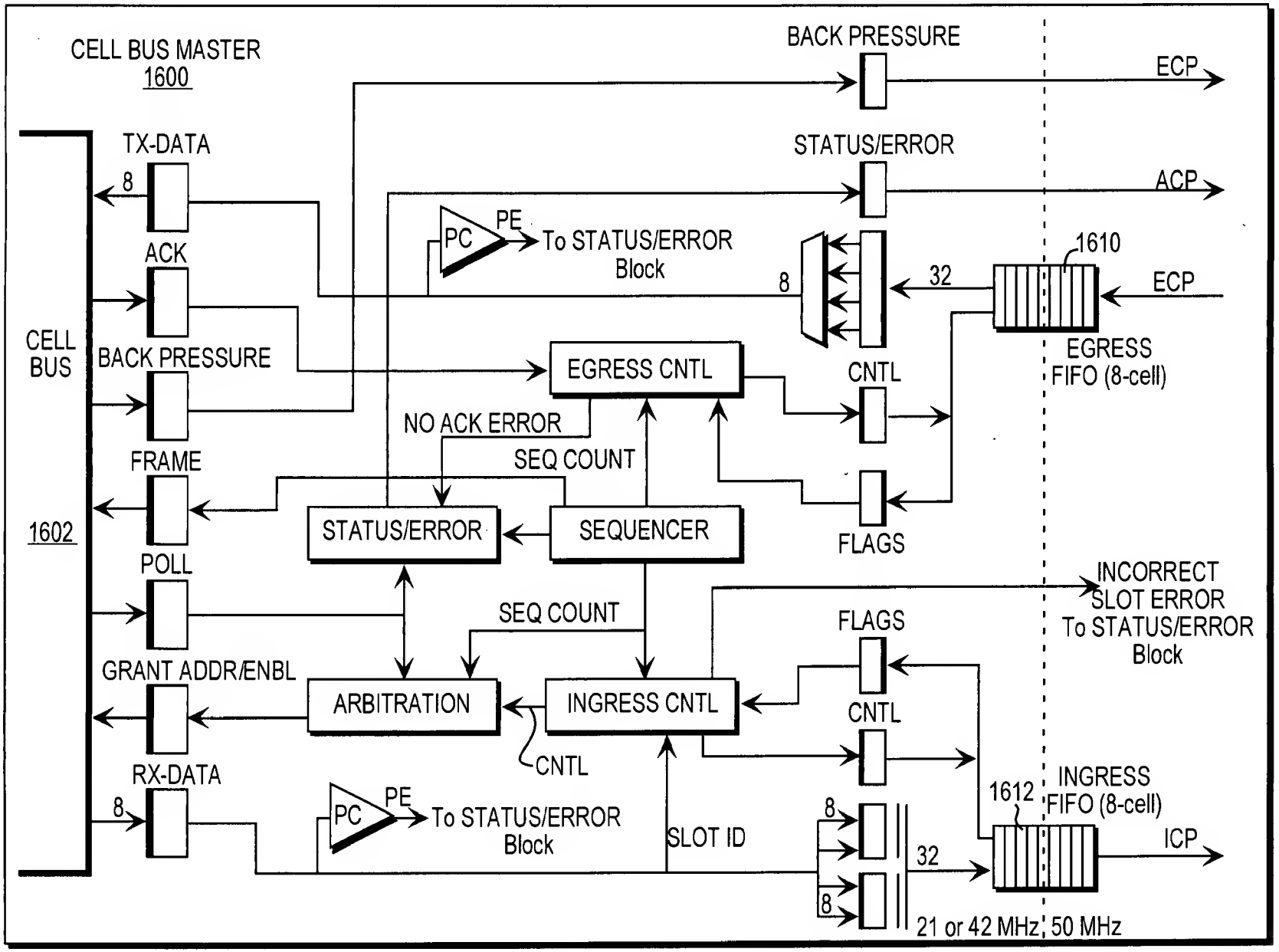


FIG. 16

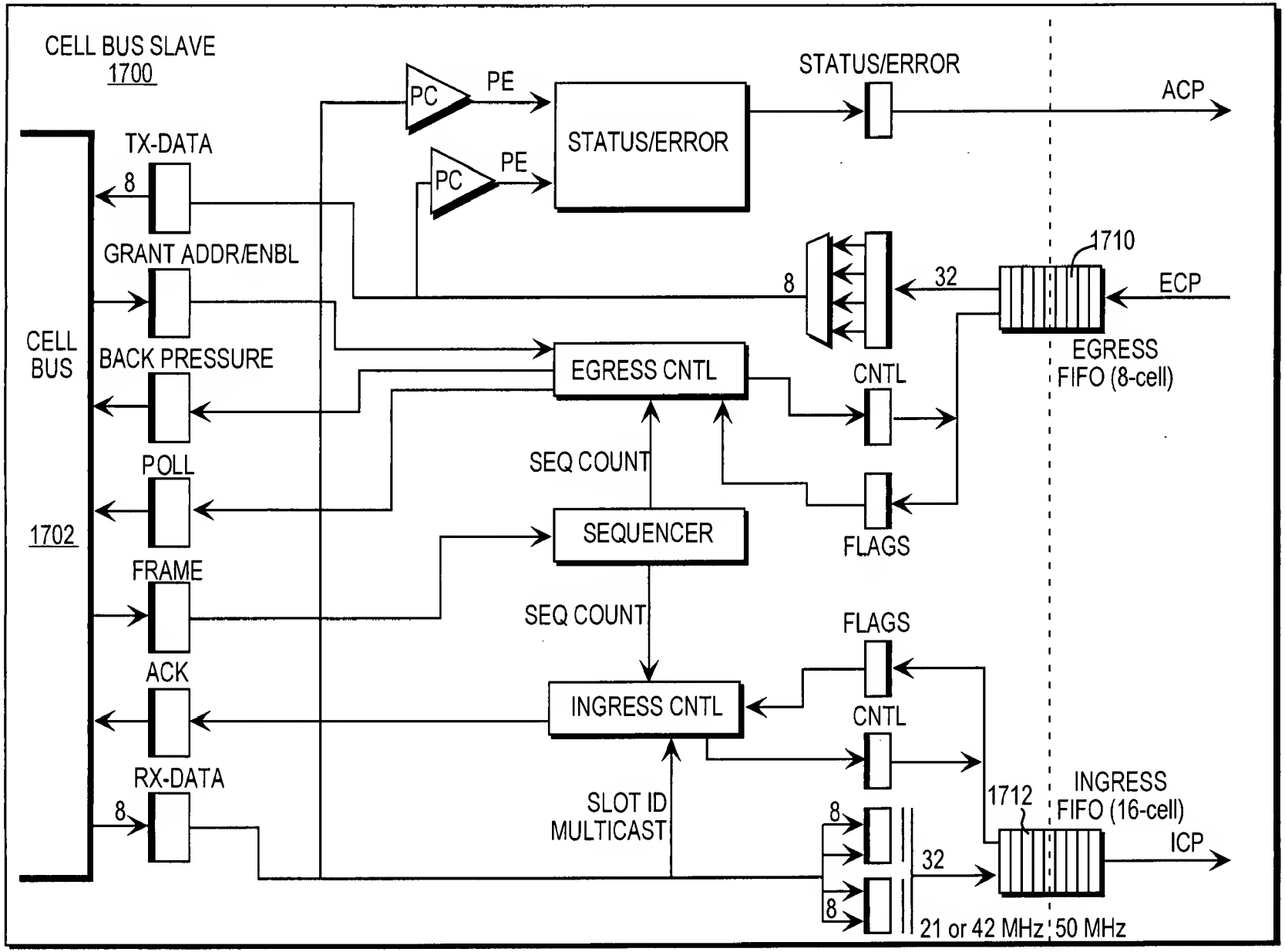


FIG. 17

| Cell Bus Cycle | TX Frame | Poll | Grant Address | Grant Enable | Reset | Tx Data (To Slave) | Rx Data (From Slave) | Ack_Lo |
|---|---|---|---|---|---|---|---|---|
| 0/58 | 1 | 0 | 0 | 1 | 0 | First Byte | 0 | 1 |
| 1 | 0 | | | 0 | | of Cell | First Byte | |
| 2 | | Odd Request | | | | Byte 2 | Byte 2 | |
| 3 | | 0 | | | | Byte 3 | Byte 3 | |
| 4 | | | | | | Byte 4 | Byte 4 | |
| 5 | | | | | | Byte 5 | Byte 5 | |
| 6-9 | | | | | | Bytes 6-9 | Bytes 6-9 | 0 (CBM checks at Cycle 18 only) |
| 10 | | Even Request | | | | Byte 10 | Byte 10 | |
| 11-14 | | 0 | | | | Bytes 11-14 | Bytes 11-14 | |
| 15 | | | Slot to Reset | Reset Type | 1 | Byte 15 | Byte 15 | |
| 16 | | | | | | Byte 16 | Byte 16 | |
| 17 | | | | | | Byte 17 | Byte 17 | |
| 18 | | Odd Ready | 0 | 0 | 0 | Byte 18 | Byte 18 | |
| 19-25 | | 0 | | | | Bytes 19-25 | Bytes 19-25 | |
| 26 | | Even Ready | | | | Byte 26 | Byte 26 | |
| 27-33 | | 0 | | | | Bytes 27-33 | Bytes 27-33 | |
| 34 | | Odd Present | | | | Byte 34 | Byte 34 | |
| 35-41 | | 0 | | | | Bytes 35-41 | Bytes 35-41 | |
| 42 | | Even Present | | | | Byte 42 | Byte 42 | |

FIG. 18

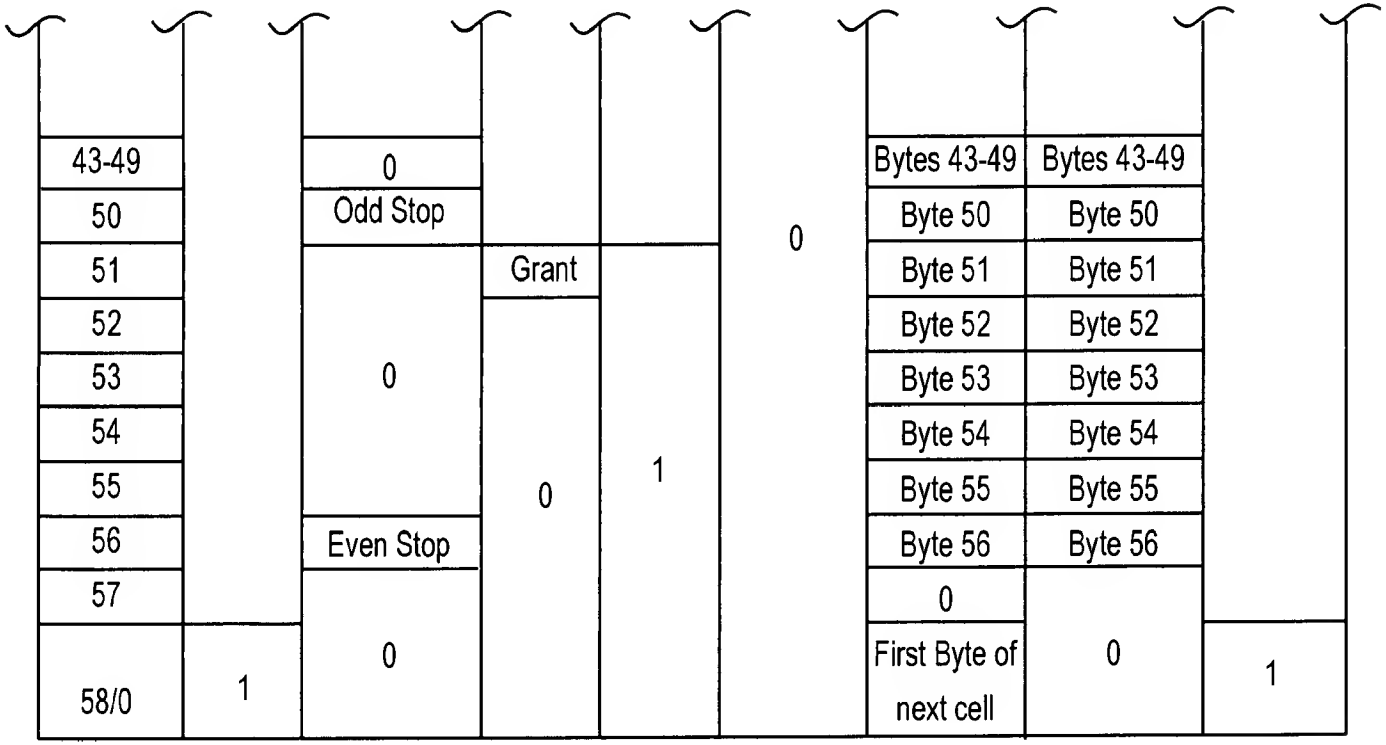


FIG. 18 (CONT.)

| Cell Bus Cycle | TX Frame | Poll | Grant Address | Grant Enable | Reset | Tx Data (From CBM) | Rx Data (To CBM) | Ack_Lo |
|---|---|---|---|---|---|---|---|---|
| 0/58 | 1 | Hi-Z | 0 | 1 | 0 | First Byte | Hi-Z | 0 |
| 1 | 0 | Odd Request | | 0 | | of Cell | First Byte | Hi-Z |
| 2 | | | | | | Byte 2 | Byte 2 | |
| 3 | | | | | | Byte 3 | Byte 3 | |
| 4 | | Hi-Z | | | | Byte 4 | Byte 4 | |
| 5 | | | | | | Byte 5 | Byte 5 | |
| 6-8 | | | | | | Bytes 6-8 | Bytes 6-8 | |
| 9 | | Even Request | | | | Byte 9 | Byte 9 | |
| 10 | | | | | | Byte 10 | Byte 10 | |
| 11 | | | | | | Byte 11 | Byte 11 | |
| 12-14 | | Hi-Z | | | | Bytes 12-14 | Bytes 12-14 | |
| 15 | | | Slot to Reset | Reset Type | | Byte 15 | Byte 15 | |
| 16 | | | | | | Byte 16 | Byte 16 | |
| 17 | | Odd Ready | | | 1 | Byte 17 | Byte 17 | |
| 18 | | | 0 | | | Byte 18 | Byte 18 | |
| 19 | | Hi-Z | | | | Byte 19 | Byte 19 | |
| 20-24 | | | | | | Bytes 20-24 | Bytes 20-24 | |
| 25 | | Even Ready | | | | Byte 25 | Byte 25 | |
| 26 | | | | | | Byte 26 | Byte 26 | |

FIG. 19

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 27 | | | | | Byte 27 | Byte 27 | |
| 27-32 | | Hi-Z | | | Bytes 27-32 | Bytes 27-32 | |
| 33 | | Odd Present | 0 | 0 | Byte 33 | Byte 33 | |
| 34 | | | | | Byte 34 | Byte 34 | 0 |
| 35 | | | | | Byte 35 | Byte 35 | |
| 35-40 | | Hi-Z | | | Bytes 35-40 | Bytes 35-40 | |
| 41 | | Even Present | | | Byte 41 | Byte 41 | |
| 42 | | | | 0 | Byte 42 | Byte 42 | |
| 43 | | | | | Byte 43 | Byte 43 | |
| 43-48 | | Hi-Z | | | Bytes 43-48 | Bytes 43-48 | |
| 49 | | Odd Stop | | | Byte 49 | Byte 49 | |
| 50 | | | | | Byte 50 | Byte 50 | |
| 51 | | | Grant | 1 | Byte 51 | Byte 51 | |
| 52 | | Hi-Z | 0 | | Byte 52 | Byte 52 | |
| 53 | | | | | Byte 53 | Byte 53 | |
| 54 | | | | | Byte 54 | Byte 54 | |
| 55 | | Even Stop | | | Byte 55 | Byte 55 | |
| 56 | | | | | Byte 56 | Byte 56 | |
| 57 | | | | | 0 | Hi-Z | |
| 58/0 | 1 | Hi-Z | | | First Byte of next cell | | |

FIG. 19 (CONT.)

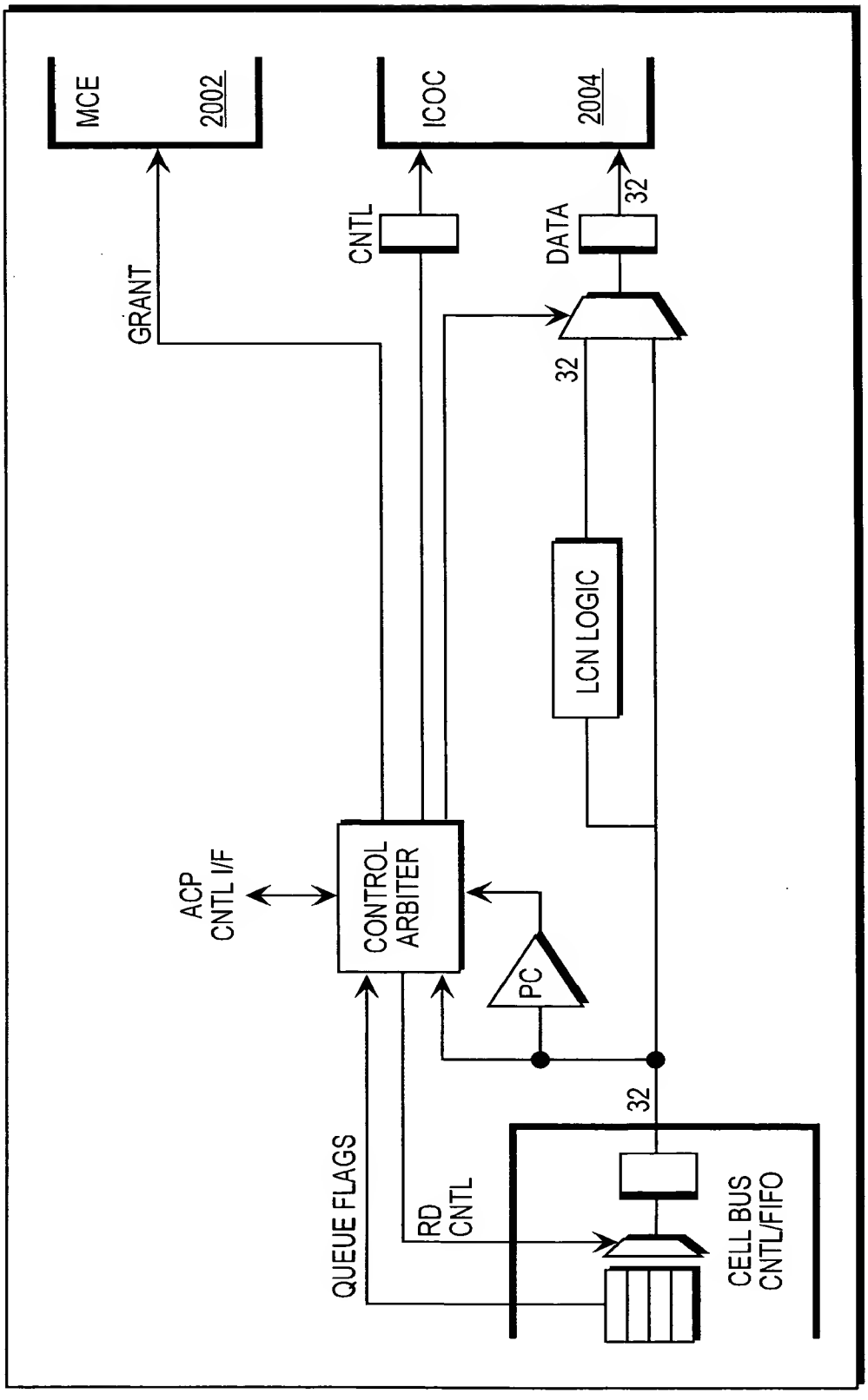


FIG. 20

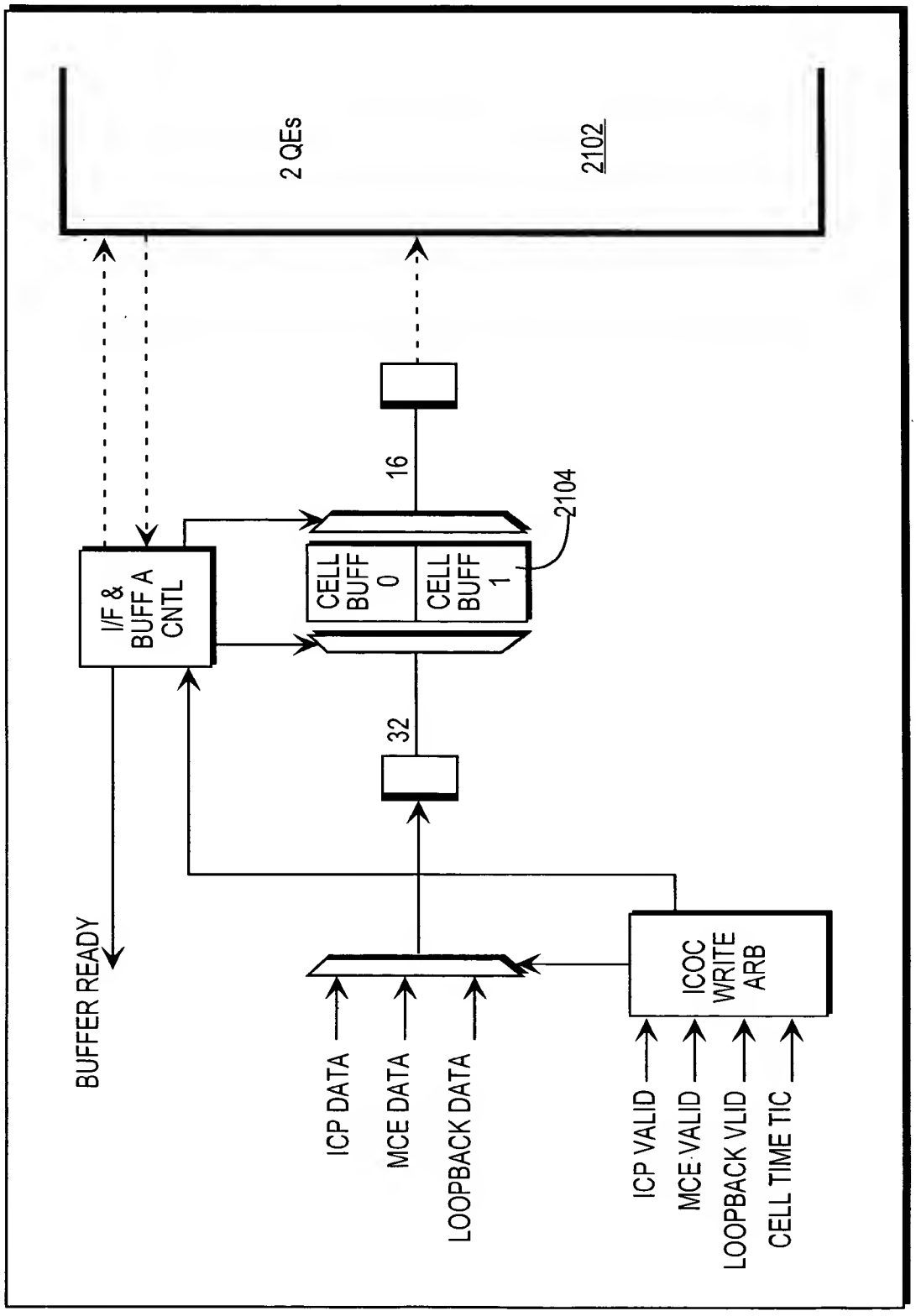


FIG. 21

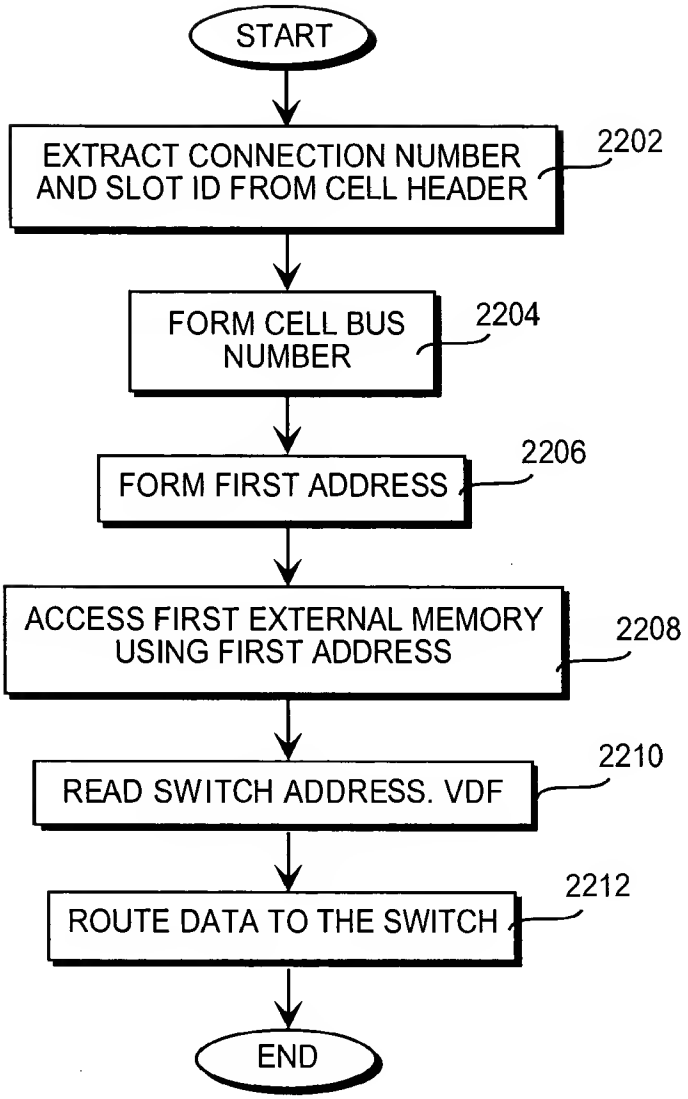


FIG. 22

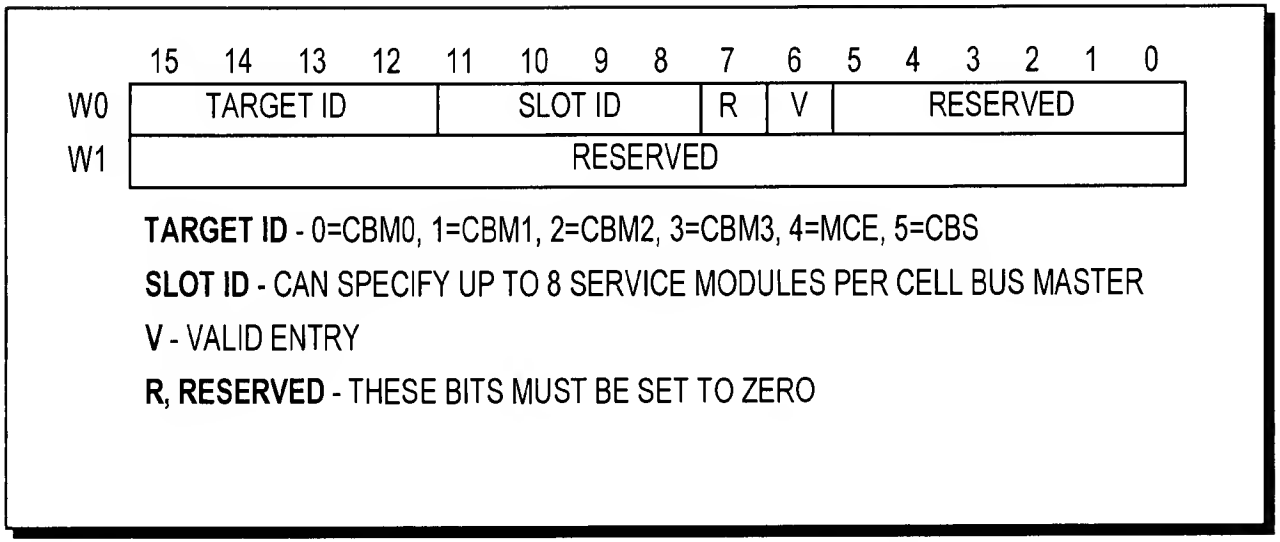


FIG. 23

| FIRMWARE INFORMATION | | | | | | | CBC HARDWARE INFORMATION | | |
|---|---|---|---|---|---|---|---|---|---|
| CBC Device Number | Device | Comment | Chassis Slot Number | Cell Bus Number | Physical Slot ID (on that Cell Bus) | QE Chip Number | CBC Chip Logic | QE Chip TX Address | Address Map RAM (Addressed by the QE TX Address) |
| 0 | SM0 | Fast or Slow SM | 1 | 0 | 1 | 0 | CBM0 | 0 | 0x01 |
| 1 | SM1 | Fast or Slow SM | 2 | 0 | 2 | 0 | CBM0 | 1 | 0x02 |
| 2 | SM2 | Fast or Slow SM | 3 | 1 | 3 | 0 | CBM1 | 2 | 0x13 |
| 3 | SM3 | Fast or Slow SM | 4 | 1 | 4 | 0 | CBM1 | 3 | 0x14 |
| 4 | SM4 | Fast or Slow SM | 5 | 2 | 5 | 0 | CBM2 | 4 | 0x25 |
| 5 | SM5 | Fast or Slow SM | 6 | 2 | 6 | 0 | CBM2 | 5 | 0x26 |
| 6 | SM6 | Slow SM only | 17 | 3 | 1 | 0 | CBM3 | 6 | 0x31 |
| 7 | SM7 | Slow SM only | 18 | 3 | 2 | 0 | CBM3 | 7 | 0x32 |
| 8 | SM8 | Slow SM only | 19 | 3 | 3 | 0 | CBM3 | 8 | 0x33 |
| 9 | SM9 | Slow SM only | 20 | 3 | 4 | 0 | CBM3 | 9 | 0x34 |
| 10 | SM10 | Slow SM only | 21 | 3 | 5 | 0 | CBM3 | 10 | 0x35 |
| 11 | SM11 | Slow SM only | 22 | 3 | 6 | 0 | CBM3 | 11 | 0x36 |

FIG. 24

| FIRMWARE INFORMATION | | | | | | | CBC HARDWARE INFORMATION | | |
|---|---|---|---|---|---|---|---|---|---|
| CBC Device Number | Device | Comment | Chassis Slot Number | Cell Bus Number | Physical Slot ID (on that Cell Bus) | QE Chip Number | CBC Chip Logic | QE Chip TX Address | Address Map RAM (Addressed by the QE TX Address) |
| 12 | MCE | Internal to CBC | N/A | N/A | N/A | 0 | MCE | 12 | 0x40 |
| 13 | Slave | Internal to CBC (RX is Connected to PSM in Slot 8, TX is NOT USED) | 8 for PSM Card in Slot 7, 7 for PSM Card in Slot 8 | N/A | N/A | 0 | CBS | 13 | NOT USED |
| 14-15 | Not Used | NOT USED | N/A | N/A | N/A | 0 | N/A | 14-15 | |
| CBC Device Number | Device | Comment | Chassis Slot Number | Cell Bus Number | Physical Slot ID (on that Cell Bus) | QE Chip Number | CBC Chip Logic | QE Chip TX Address | Address Map RAM (Addressed by the QE TX Address) |

FIG. 24 (CONT.)

| FIRMWARE INFORMATION | | | | | | | CBC HARDWARE INFORMATION | | |
|---|---|---|---|---|---|---|---|---|---|
| CBC Device Number | Device | Comment | Chassis Slot Number | Cell Bus Number | Physical Slot ID (on that Cell Bus) | QE Chip Number | CBC Chip Logic | QE Chip TX Address | Address Map RAM (Addressed by the QE TX Address) |
| 16 | SM0 | Fast or Slow SM | 9 | 4 | 9 | 1 | CBM0 | 0 | 0x09 |
| 17 | SM1 | Fast or Slow SM | 10 | 4 | 10 | 1 | CBM0 | 1 | 0x0A |
| 18 | SM2 | Fast or Slow SM | 11 | 5 | 11 | 1 | CBM1 | 2 | 0x1B |
| 19 | SM3 | Fast or Slow SM | 12 | 5 | 12 | 1 | CBM1 | 3 | 0x1C |
| 20 | SM4 | Fast or Slow SM | 13 | 6 | 13 | 1 | CBM2 | 4 | 0x2D |
| 21 | SM5 | Fast or Slow SM | 14 | 6 | 14 | 1 | CBM2 | 5 | 0x2E |
| 22 | SM6 | Slow SM only | 25 | 7 | 9 | 1 | CBM3 | 6 | 0x39 |
| 23 | SM7 | Slow SM only | 26 | 7 | 10 | 1 | CBM3 | 7 | 0x3A |
| 24 | SM8 | Slow SM only | 27 | 7 | 11 | 1 | CBM3 | 8 | 0x3B |
| 25 | SM9 | Slow SM only | 28 | 7 | 12 | 1 | CBM3 | 9 | 0x3C |
| 26 | SM10 | Slow SM only | 29 | 7 | 13 | 1 | CBM3 | 10 | 0x3D |
| 27 | SM11 | Slow SM only | 30 | 7 | 14 | 1 | CBM3 | 11 | 0x3E |
| 28 | MCE | Internal to CBC | N/A | N/A | N/A | 1 | MCE | 12 | 0x40 |
| 29 | Slave | Internal to CBC NOT USED | N/A | N/A | N/A | 1 | CBS | 13 | NOT USED |
| 30-31 | Not Used | NOT USED | N/A | N/A | N/A | 1 | N/A | 14-15 | NOT USED |

FIG. 25

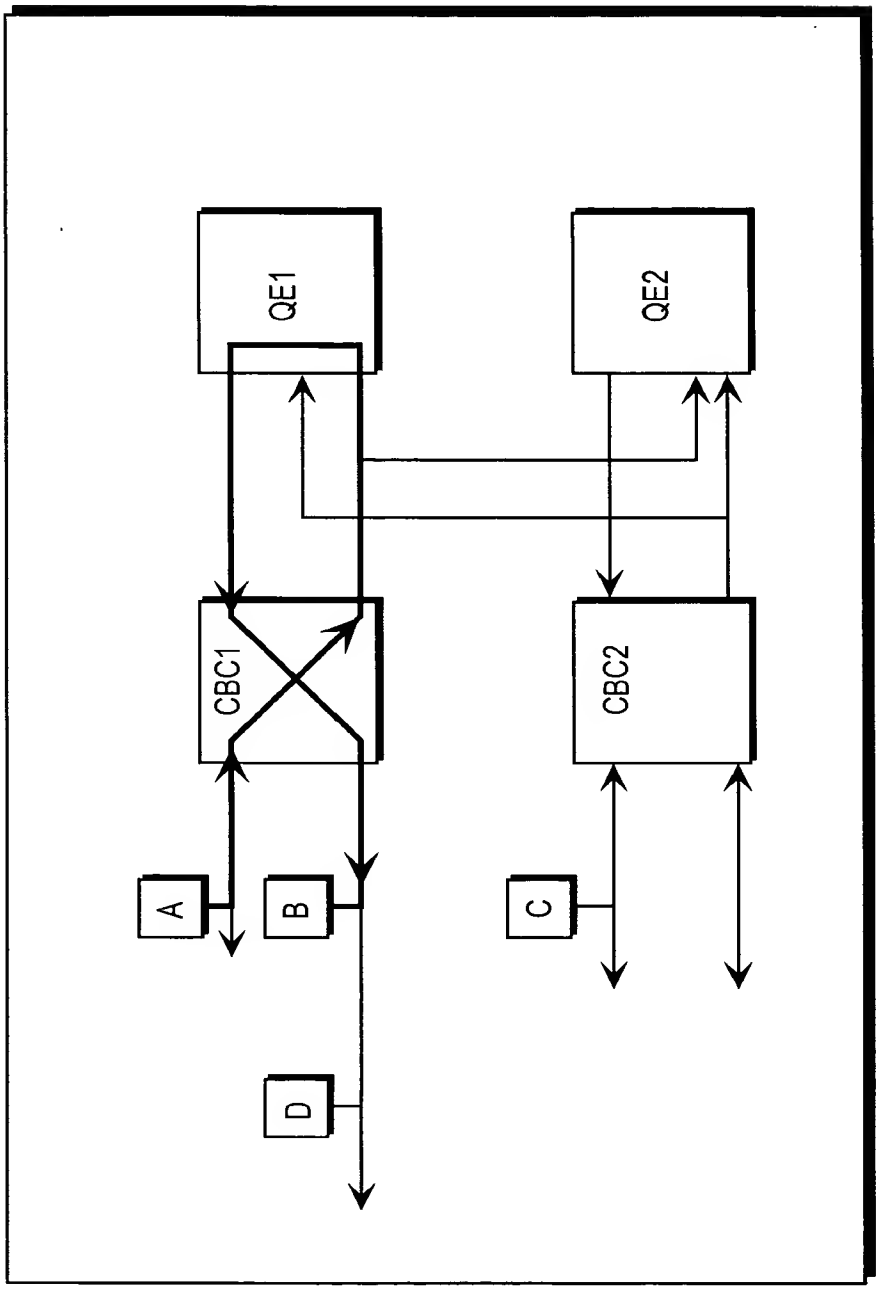


FIG. 26

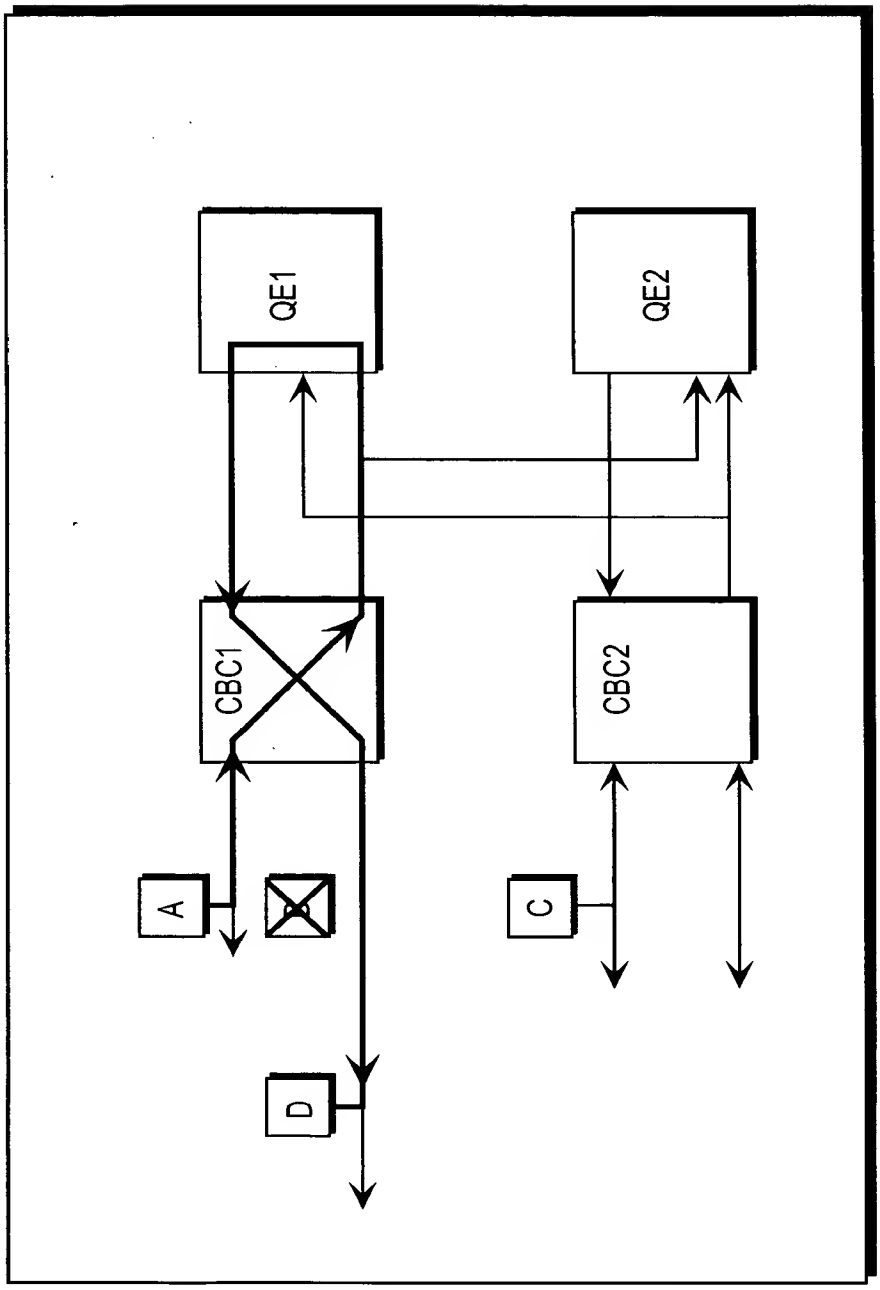


FIG. 27

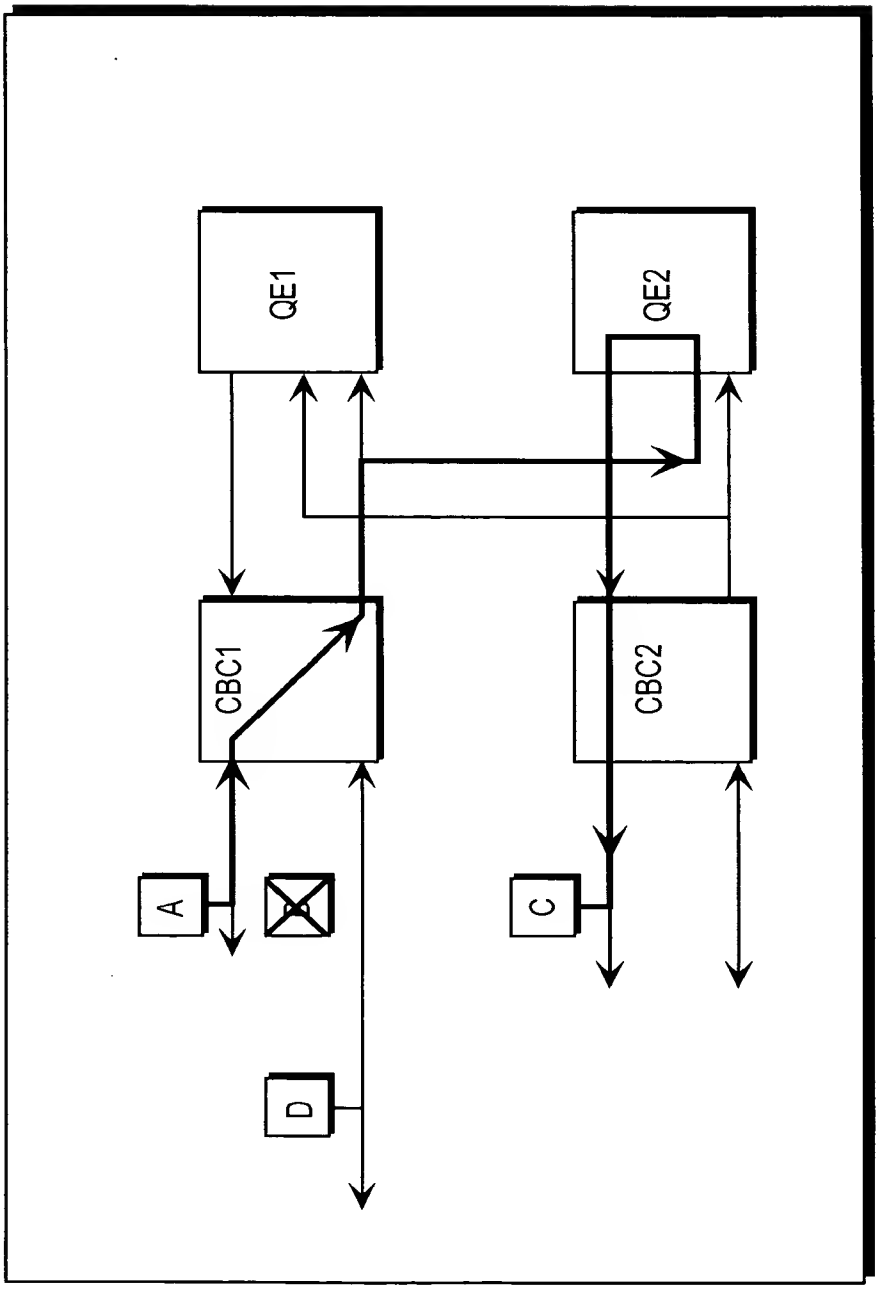


FIG. 28

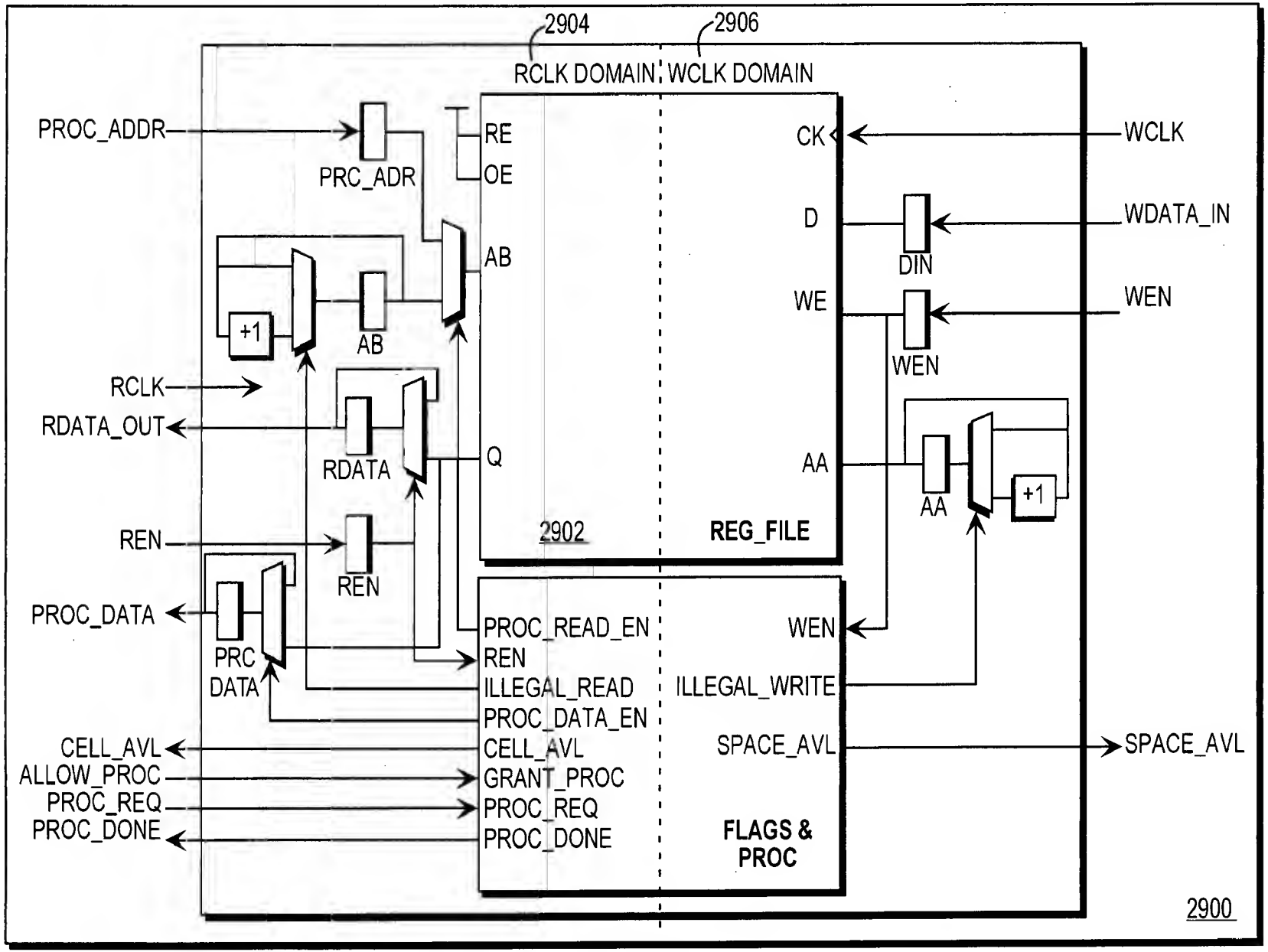


FIG. 29

| PARAMETER | PURPOSE | CBM Egress FIFO | CBM Ingress FIFO | CBS Ingress FIFO |
|---|---|---|---|---|
| num_bits_in_fifo_word | Number of bits in each FIFO word | 34 | 34 | 34 |
| num_words_in_cell | Number of words in one cell | 14 | 14 | 14 |
| log2_num_words_in_cell | Minimum bits needed to represent num_words_in_cell | 4 | 4 | 4 |
| num_cells_in_fifo | Number of cells in the FIFO | 8 | 8 | 16 |
| log2_num_cells_in_fifo | Minimum bits needed to represent num_cells_in_fifo | 3 | 3 | 4 |
| log2_num_words_in_fifo | Number of bits in FIFO address | 7 | 7 | 8 |
| wclk_2_rclk_ratio | WCLK to RCLK frequency ratio (minimum = 1) - WCLK=50 MHZ RCLK=21 MHZ RATIO=3 WCLK=21 MHZ RCLK=50 MHZ RATIO=1 | 3 | 1 | 1 |
| rclk_2_wclk_ratio | RCLK to WCLK frequency ratio (minimum = 1) - RCLK=50 MHZ WCLK=21 MHZ RATIO=3 RCLK=21 MHZ WCLK=50 MHZ RATIO=1 | 1 | 3 | 3 |

FIG. 30

| NAME | COUNT | DIRECTION | COMMENTS |
|---|---|---|---|
| **Write Port Interface** | | | |
| write_clk_i | 1 | Input | Write Port Clock |
| wclk_reset_i | 1 | Input | Write Port Reset |
| write_data_i | num_bits_in_fifo_word | Input | Write Data Input |
| write_en_i | 1 | Input | Write Enable |
| write_cell_cntr_o | log2_num_cells_in_fifo | Output | Write Port Cell Count |
| cell_space_avail_o | 1 | Output | Room for at least one more cell |
| **Read Port Interface** | | | |
| read_clk_i | 1 | Input | Read Port Clock |
| rclk_reset_i | 1 | Input | Read Port Reset |
| read_data_o | num_bits_in_fifo_word | Output | Read Data Output |
| read_en_i | 1 | Input | Read Enable |
| read_cell_cntr_o | log2_num_cells_in_fifo | Output | Read Port Cell Count |
| cell_avail_o | 1 | Output | At least one more cell in FIFO |
| allow_proc_read_i | 1 | Input | Granting Processor Port for reading; When the allow_proc_read_i is asserted, the Read Port is not allowed to read. In addition, the next 2 cycles following the last cycle the allow_proc_read_i is asserted are also not available. |
| **Processor Port Interface** | | | |

FIG. 31

| NAME | COUNT | DIRECTION | COMMENTS |
|---|---|---|---|
| proc_read_req_i | 1 | Input | Processor request read operation |
| proc_read_adrs_i | log2_num_words_in_fifo | Input | Processor read address |
| proc_read_data_o | num_bits_in_fifo_word | Output | Processor read data |
| proc_read_done_o | 1 | Output | Processor read request completed |
| **BIST Interface** | | | |
| bist_test_i | 1 | Input | |
| bist_cntl_i | 1 | Input | |
| brt_flag_o | 1 | Output | |
| bist_complete_o | 1 | Output | |

FIG. 31 (CONT.)

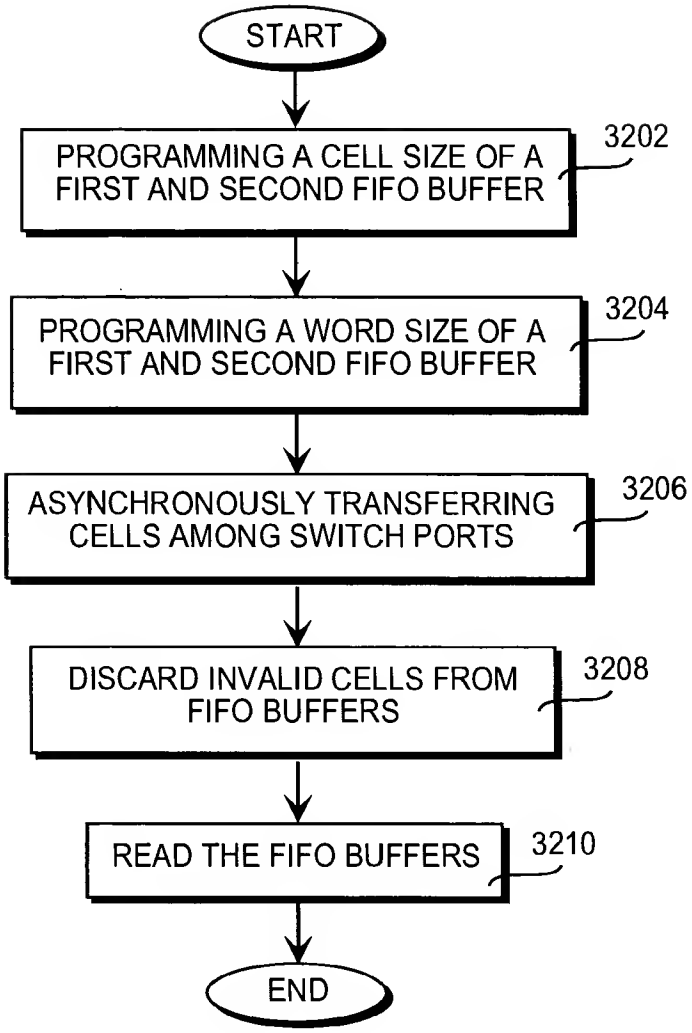


FIG. 32

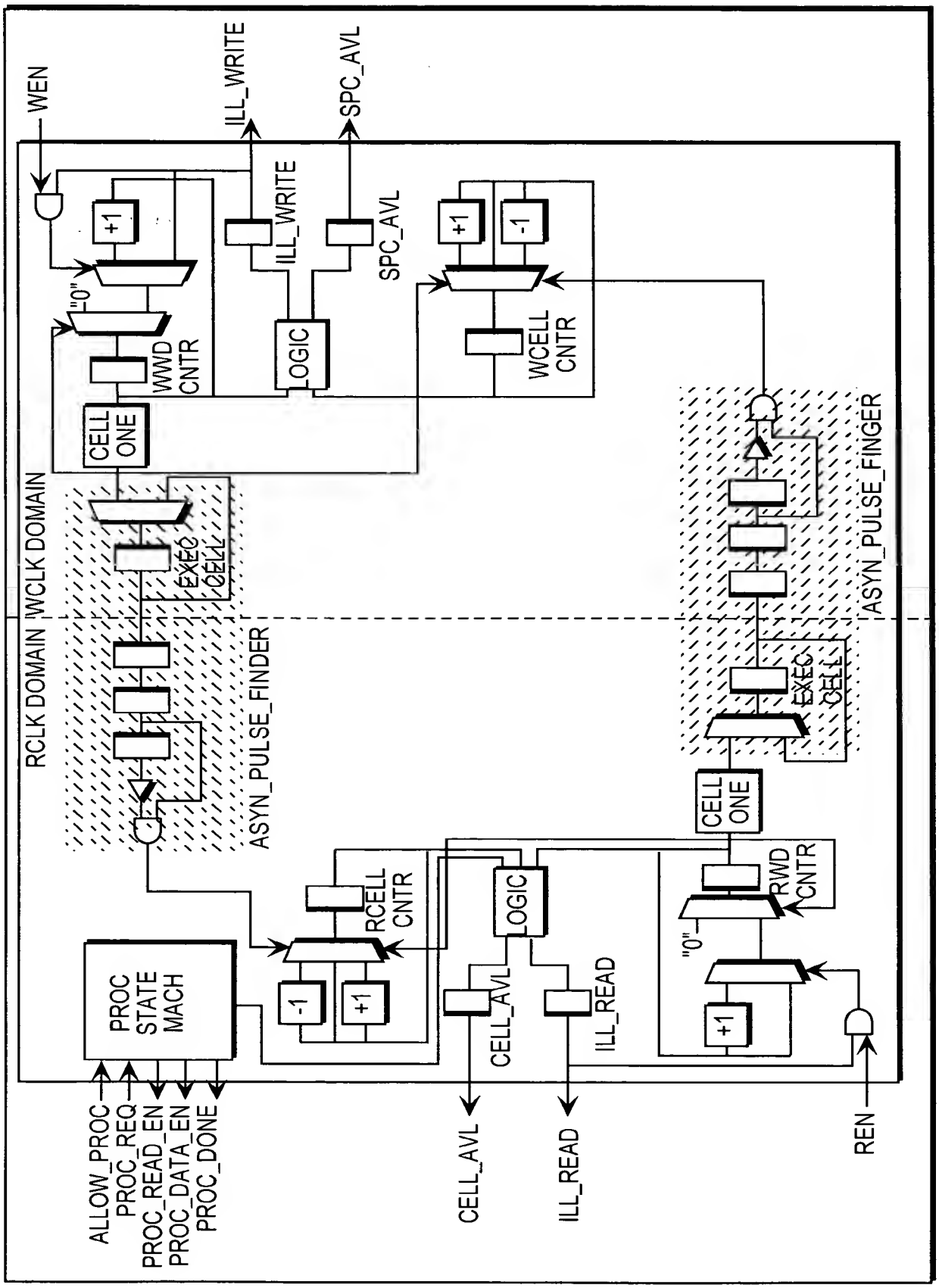


FIG. 33

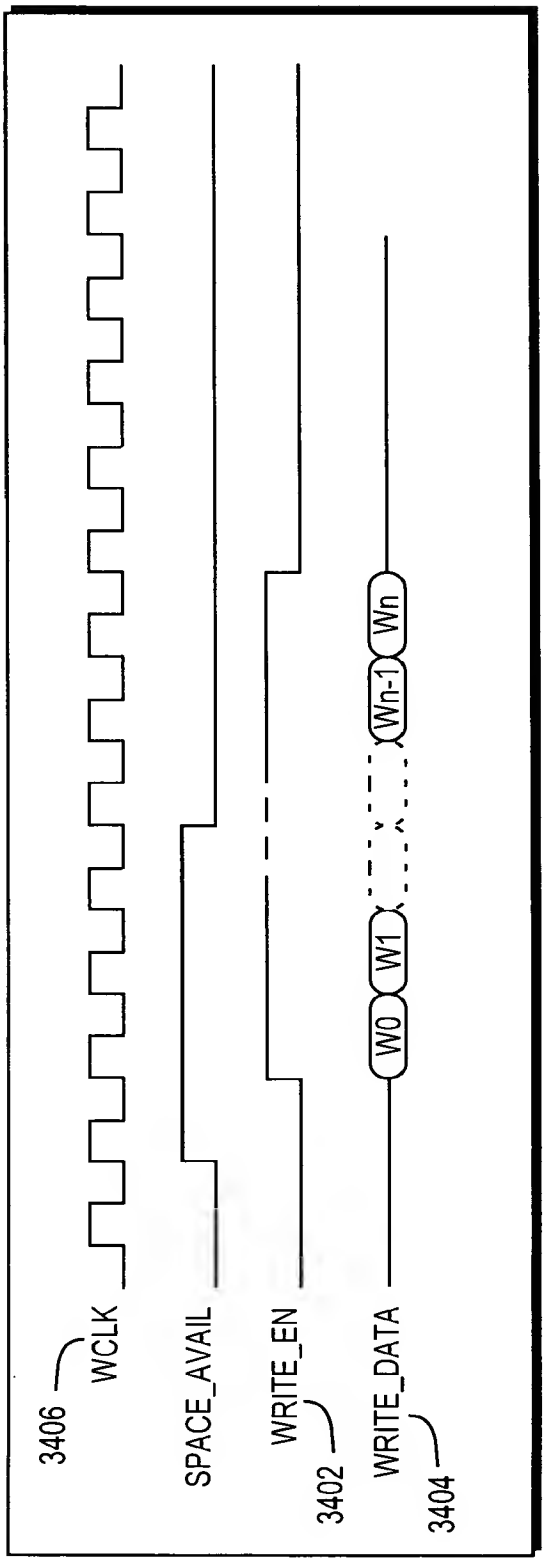


FIG. 34

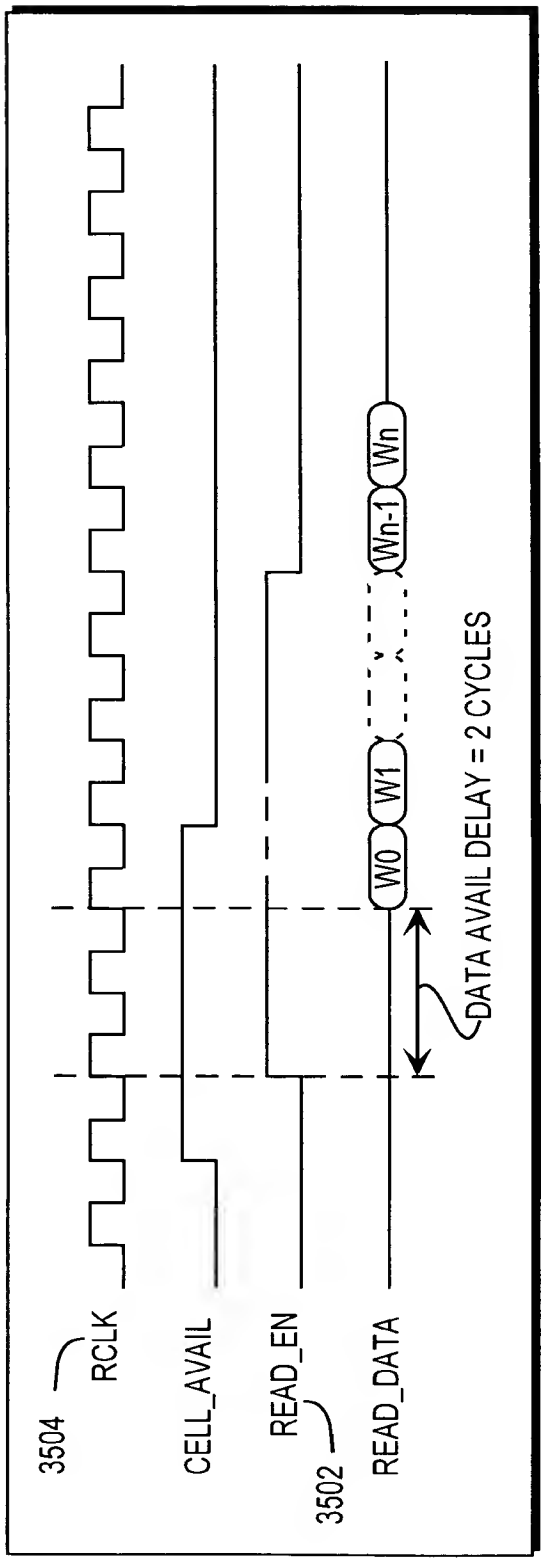


FIG. 35

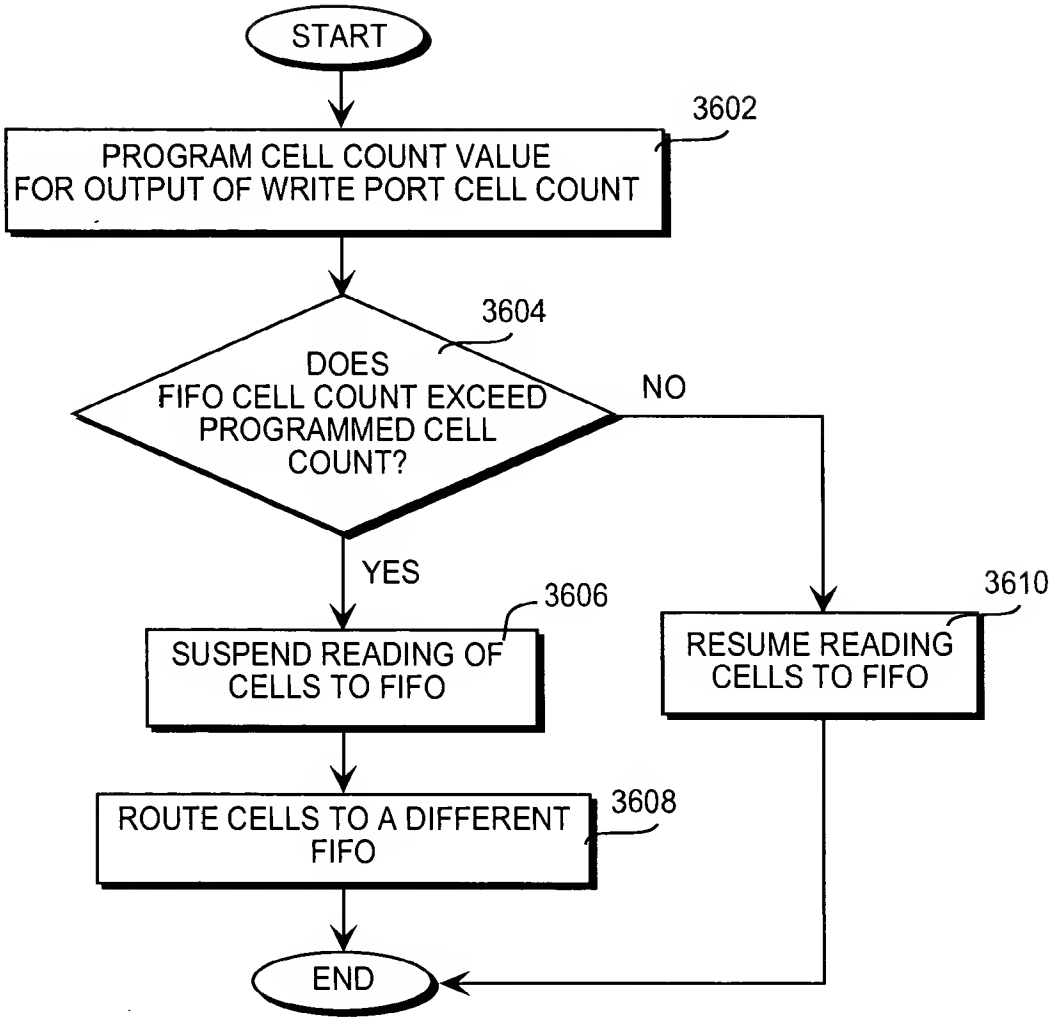


FIG. 36

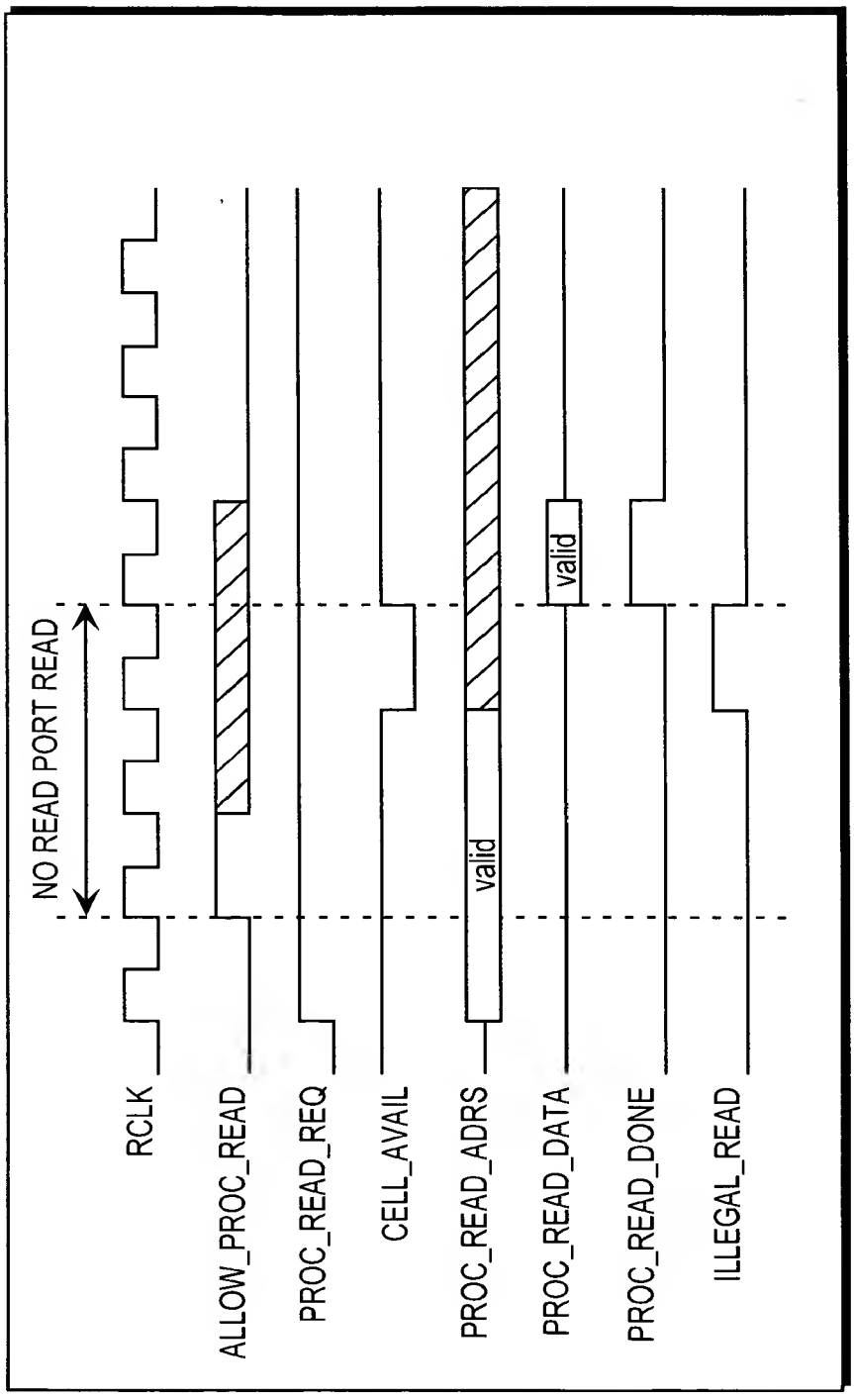


FIG. 37

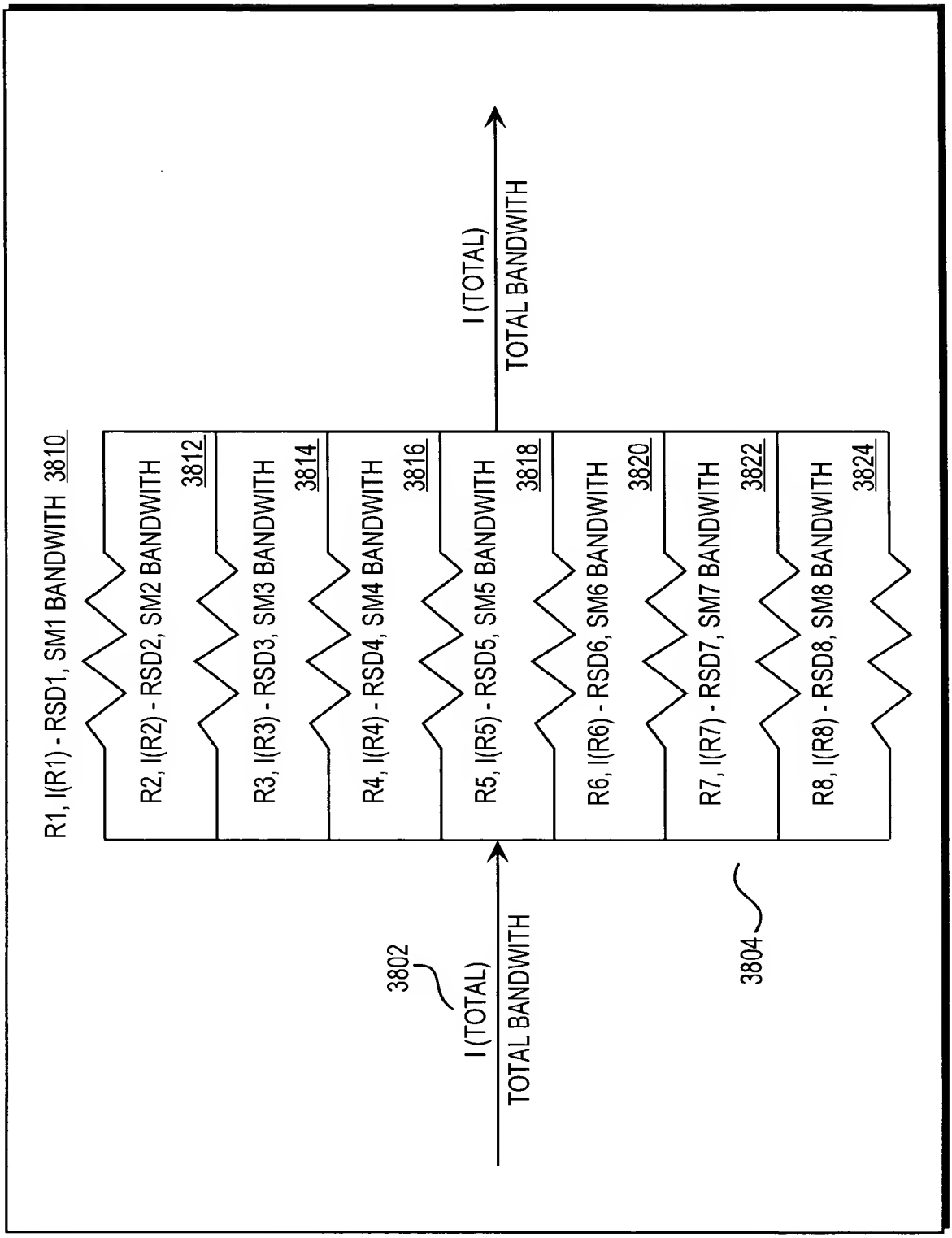


FIG. 38

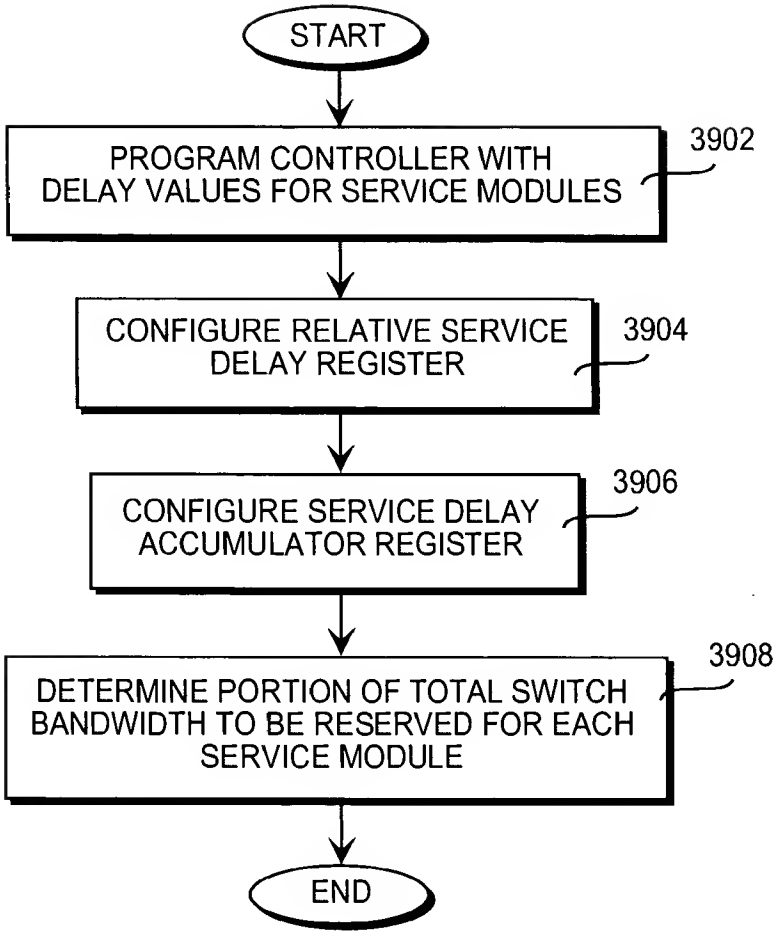


FIG. 39

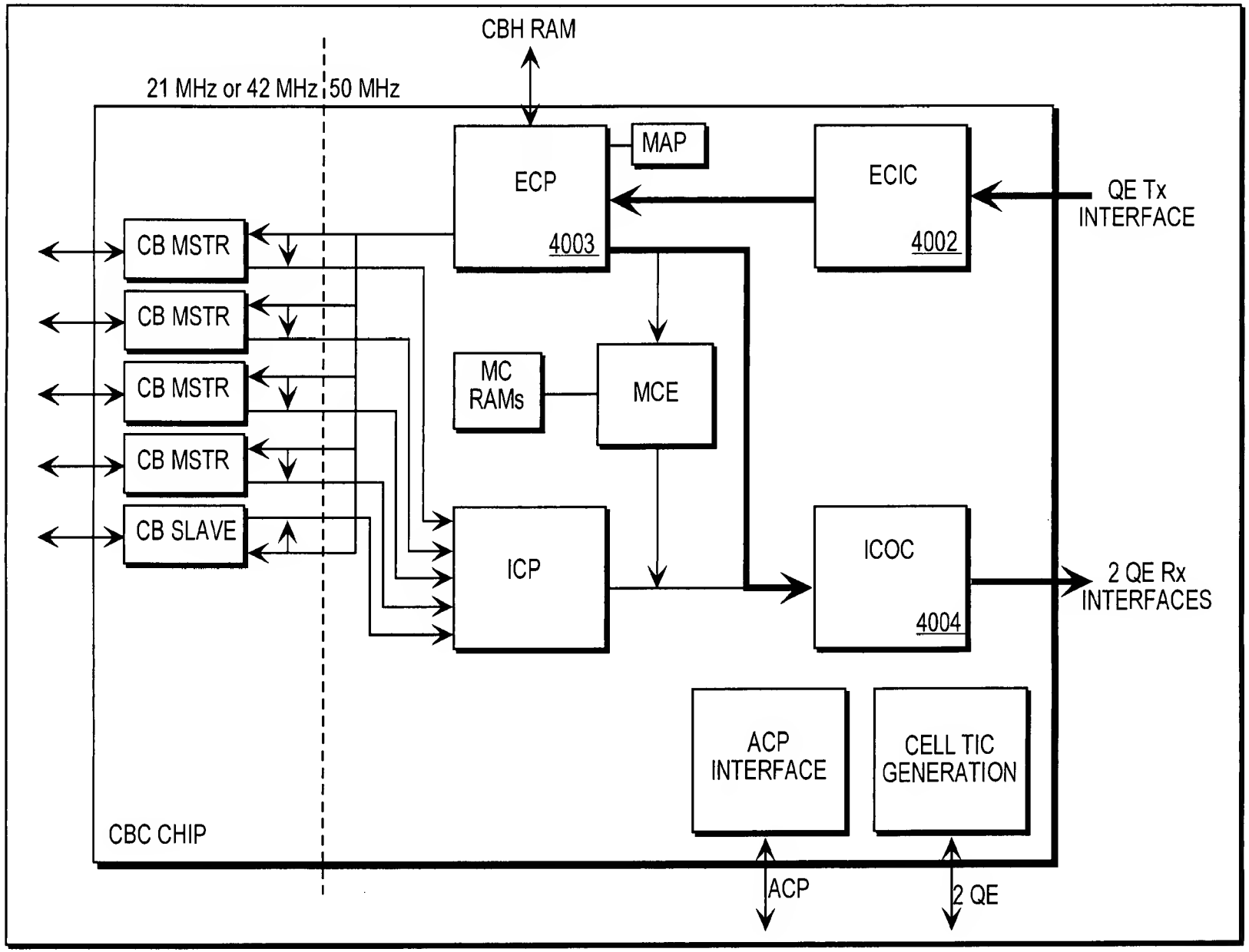


FIG. 40

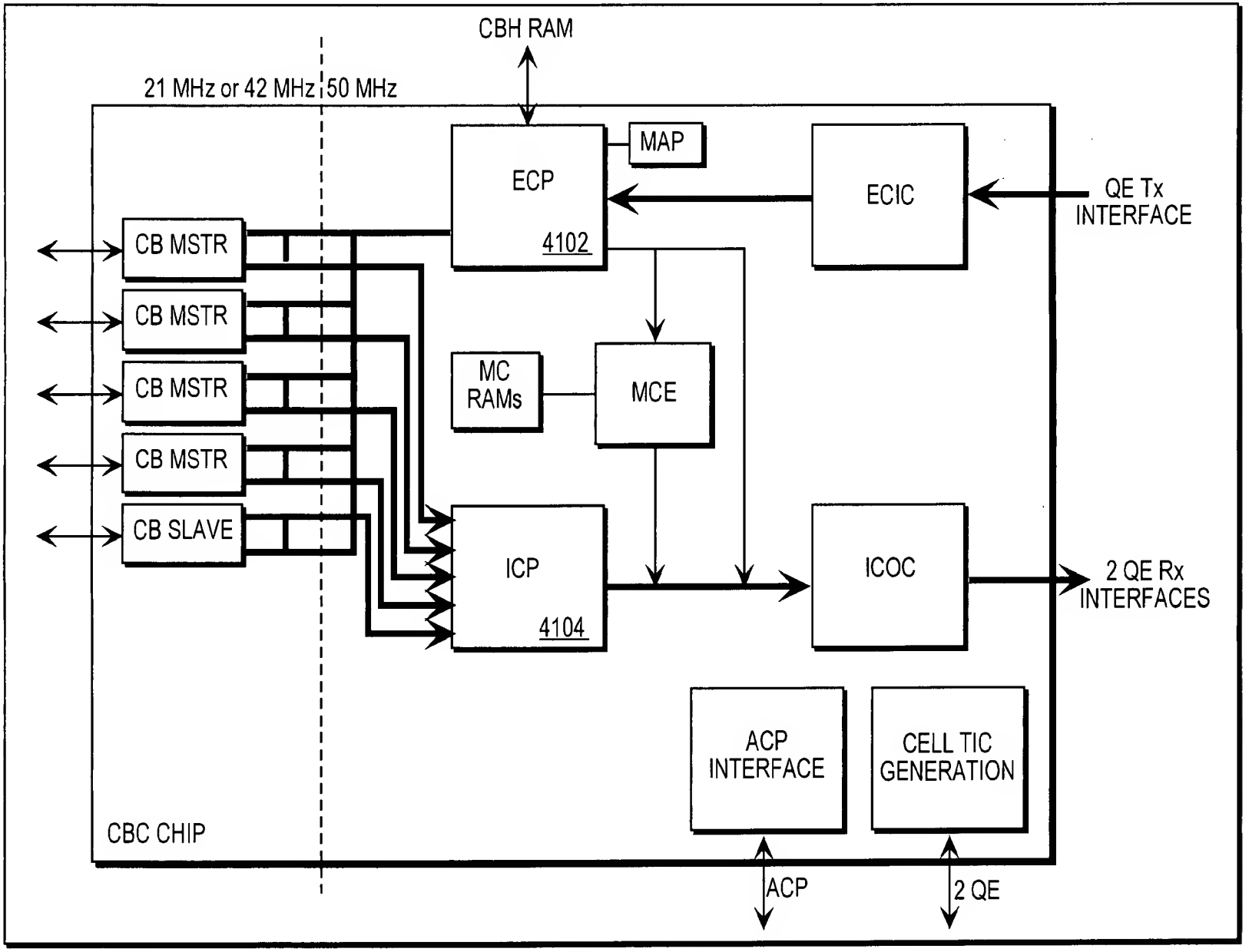


FIG. 41